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Market Overview

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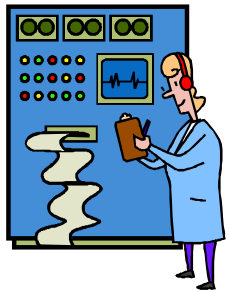
Computing System Evolution
From Mainframes to desktop to HPC

- **Mainframes ~ 1965**
  - Tightly coupled processor, computer, OS and software from a single company
  - Proprietary software
  - >$1M



- **Departmental Minicomputers ~ 1970**
  - Enables significant proliferation of servers as machines leave glass houses
  - <$1M

- **RISC Processors and UNIX ~1976**
  - The beginning of “Commodity Computer Market”
  - Processor, Computer and Software begin to un-bundle
  - A proliferation of new companies (SUN, MIPS, SGI) with the promise of significantly improved performance
    - DEC Alpha in early 90’s outperforms PC processor by 2X

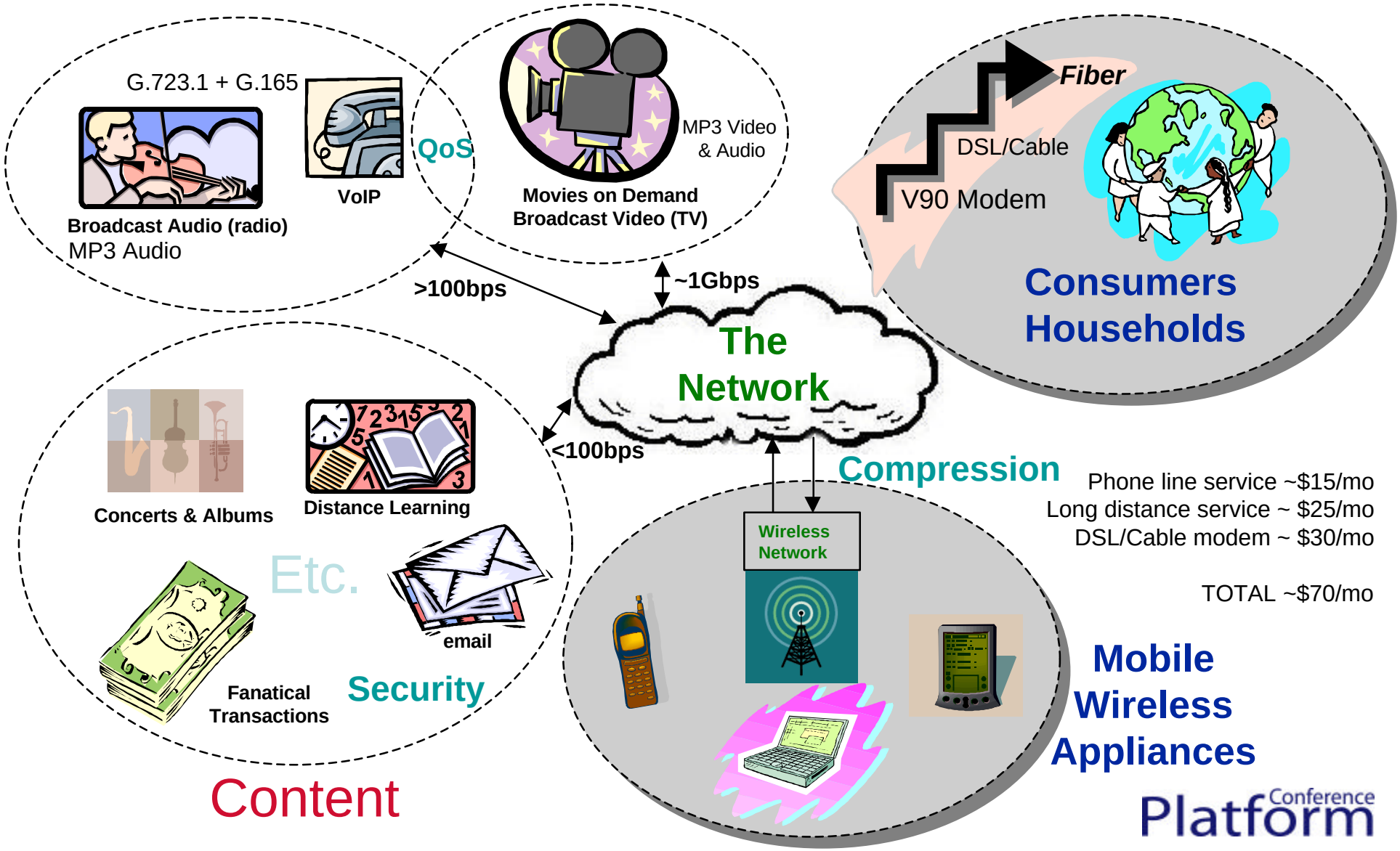
- **Centralized HPC ~ 1995**
  - The re-introduction of a centralized HPC cluster

X86-32 Commodity Computing

- **Even before the turn of the century, Desktop & Mobile PCs have become a commodity market**
  - ✓ AMD drove the 2GHz PC to the sub $1k price range
  - ✓ Desk Top Systems from different OEMs are basically the same:
    - Processor, chipset,
    - motherboard,
    - Peripheral mix,
    - power supply and chassis
    - Only the branding was different.
- **Most Workstations are simply a high-performance desktop PC with two or more processors**
- **Windows® and Linux have similarly transformed the OS business**
- **Pricing Trends**
  - ✓ ***Pay for service* - business model**
- **Technology trends –** "By the end of this decade, we will see a convergence to IP packet based content delivery for all of our voice, video and data."

  - Gene A Frantz, Principal Fellow, Texas Instruments.

Convergence in the Communications Market



The x86 Revolution

- **Performance**
  - By ‘97 the AMD Athlon™ & Intel® Pentium® III™ erased any performance advantage of RISC
- **Application Software**
  - Price, quantity and quality of x86 software *dominated Workstation* and now *Server* applications
- **Operations Systems**
  - Windows® and Linux have emerged as the “standard” for x86
- **Networked PCs**
  - The x86 architecture combined with today's high speed/low cost Networking advances has enabled distributed and clustered processing
- **Multiprocessing & High Performance Computing (HPC)**
  - The x86 has dominated 1P & 2P server space. The x86 has become the preferred processor for 1U and 2U as well as blade server architecture
  - The availability of 4P and larger x86 system architectures, combined with advanced clustering topologies are driving the next generation of HPC server applications

The AMD Opteron™ Revolution

AMD's Eighth Generation Processor Family is designed to!

- **Performance**
  - Significantly *increase system performance* over current State-of-art using non-exotic silicon process and common sense design techniques.
- **Application Software**
  - Will leverage the existing x86-32 installed software base - 100% compatibility
- **Operations Systems**
  - Runs Windows® and Linux - with 64 bit versions coming

- **Networked PCs**
  - Enable the next generation of Networking systems - drive down the cost of servers, distributed and clustered processing systems with volumes of *millions per quarter*
- **Multiprocessing & High Performance Computing (HPC)**
  - Raise the bar - Enable the 4P and 8P server markets
  - Drive the *data center processor* to a commodity market
    - Scale out with small form factor (1U Rack Mount and Blade Servers)
    - Scale up with multi processor and cluster computing
      - Initially up to 8P glue less Multi Processor systems, Later >8P with switches
      - HPC

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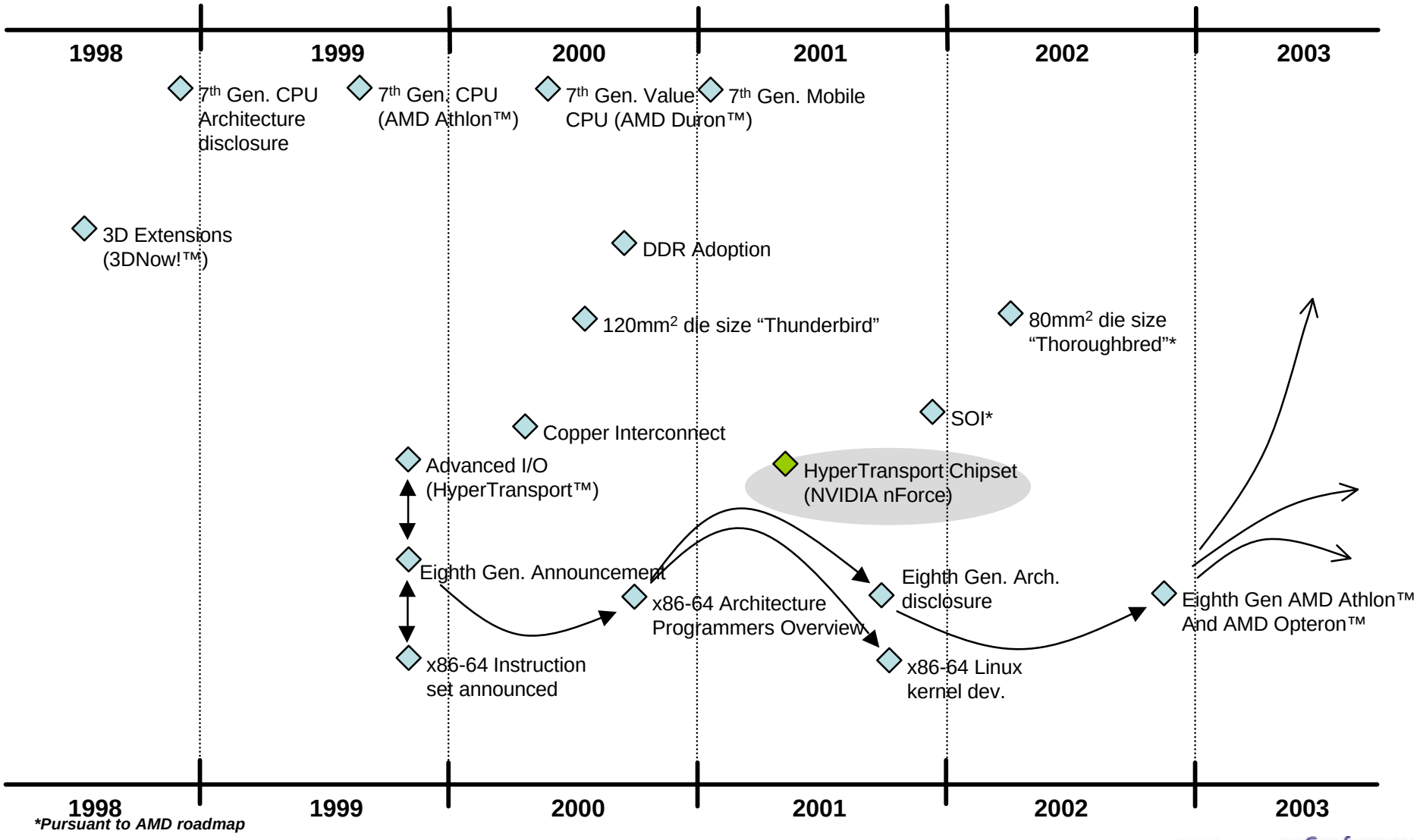
AMD Opteron™ Impact on High End Computing

- **Eliminate the world of fractured proprietary CPU/OS combinations**
  - Alpha/TRU64
  - Power4/AIX
  - UltraSPARC/Solaris
  - PA-RISC/HP-UX
- **Converge onto x86-64 Windows® and/or Linux™**
- **Standards**
  - Lower cost systems -> volume
  - Straightforward world for ISVs
  - Commodity infrastructure
- **AMD Opteron™ yields *low risk and low cost of ownership* with investment protection**

AMD's Innovations Timeline



**Pursuant to AMD roadmap*

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The HyperTransport™ Technology Consortium

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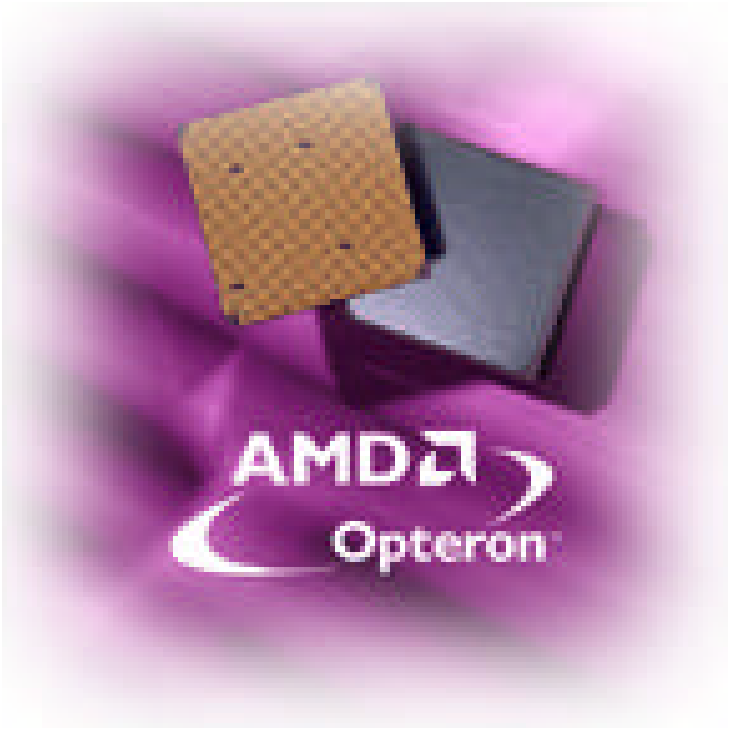
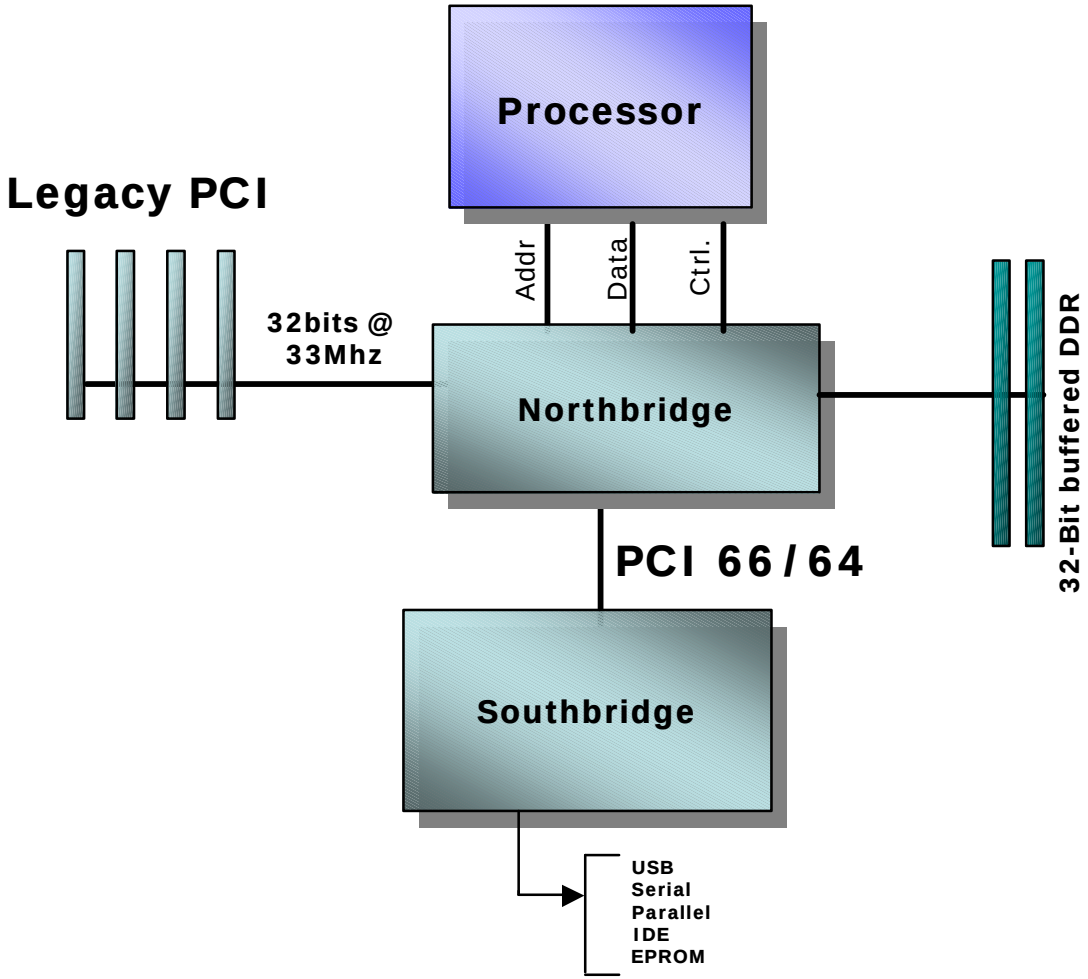
AMD Opteron™ & Eighth Generation AMD Athlon™ Family Processors Overview

AMD's Opteron™ Family Processors

- Overview of AMD Eighth generation x86-64 processor Family: AMD Athlon™ & AMD Opteron™
  - CPU
    - Cache & Branch Prediction
    - Northbridge
  - Electrical and Physical issues
  - Multi-Processing Interface
  - Summary



State of Art Desk Top System

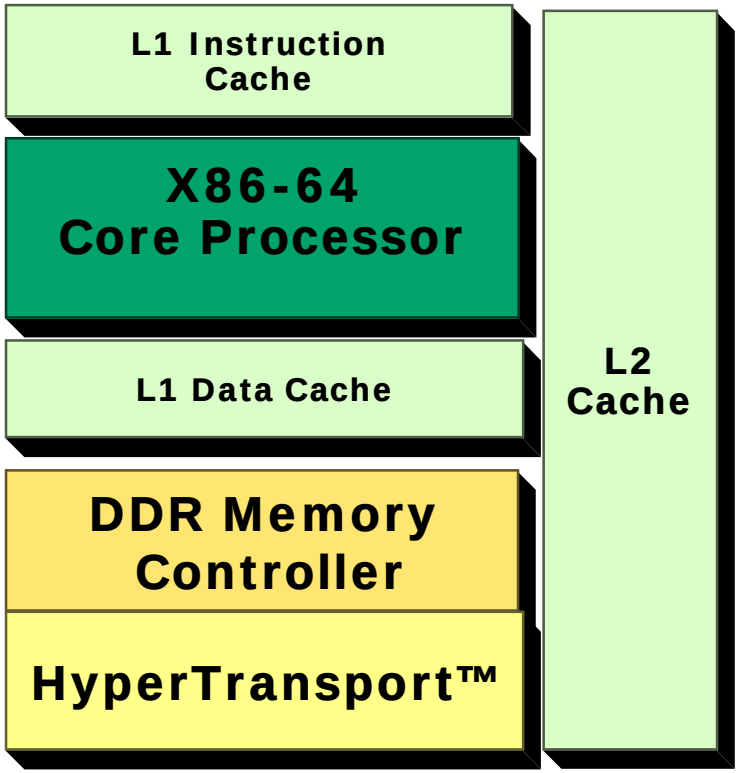


System Weaknesses

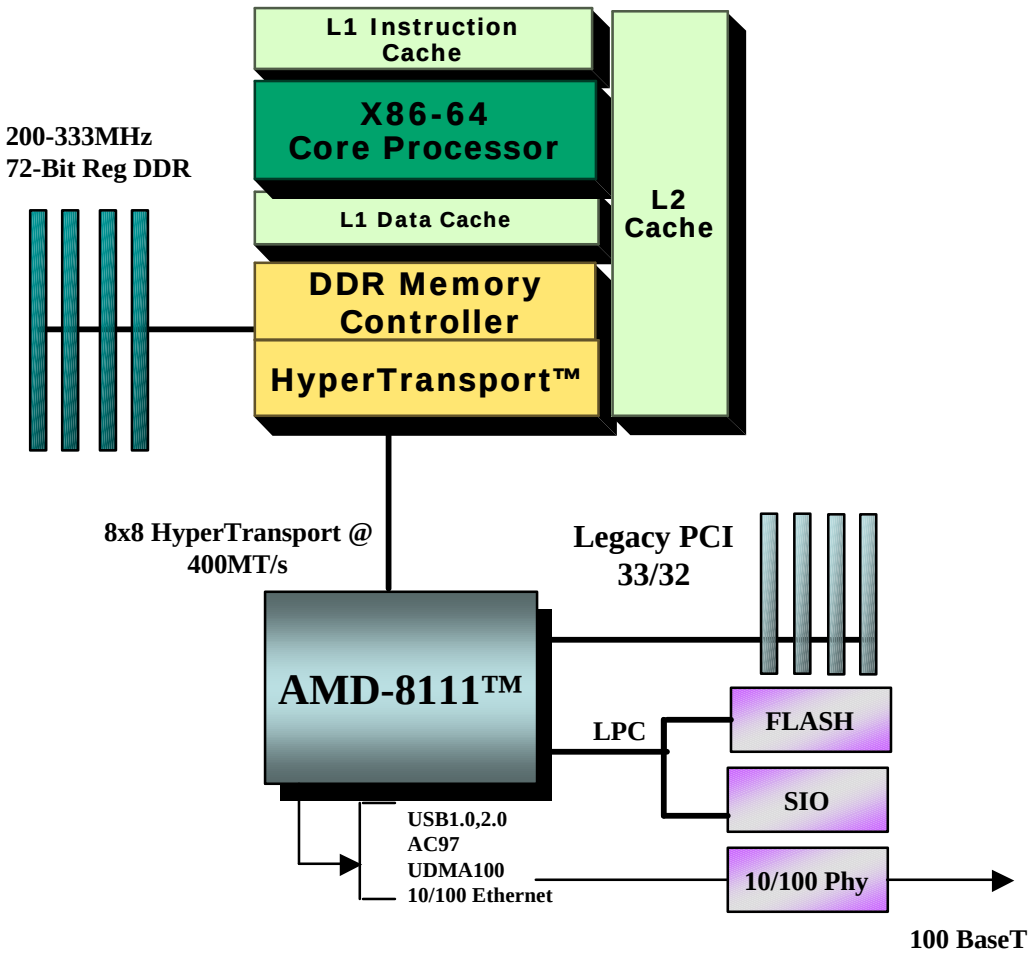
- Memory Latency and Bandwidth
- I/O Latency and Bandwidth ~1Gb
- Doesn't easily support a multiprocessing architecture

AMD Athlon™ & AMD Opteron™ Feature set

- 64 bit x86 instruction set
  - ✓ 100% backwards compatible with installed legacy x86-32bit Software
  - ✓ CPU is Evolutionary not Revolutionary
- Bigger, Faster, Smarter L1 & L2 Cache
  - ✓ Not just bigger but real cycle for cycle performance improvements over AMD Athlon™ XP
- Integrated Northbridge
  - ✓More reliable
  - ✓Lower power
  - ✓*Faster*
- Integrated HyperTransport™ I/O
  - ✓ >10x through of PCI 33/32
  - ✓ Glueless multiprocessor support



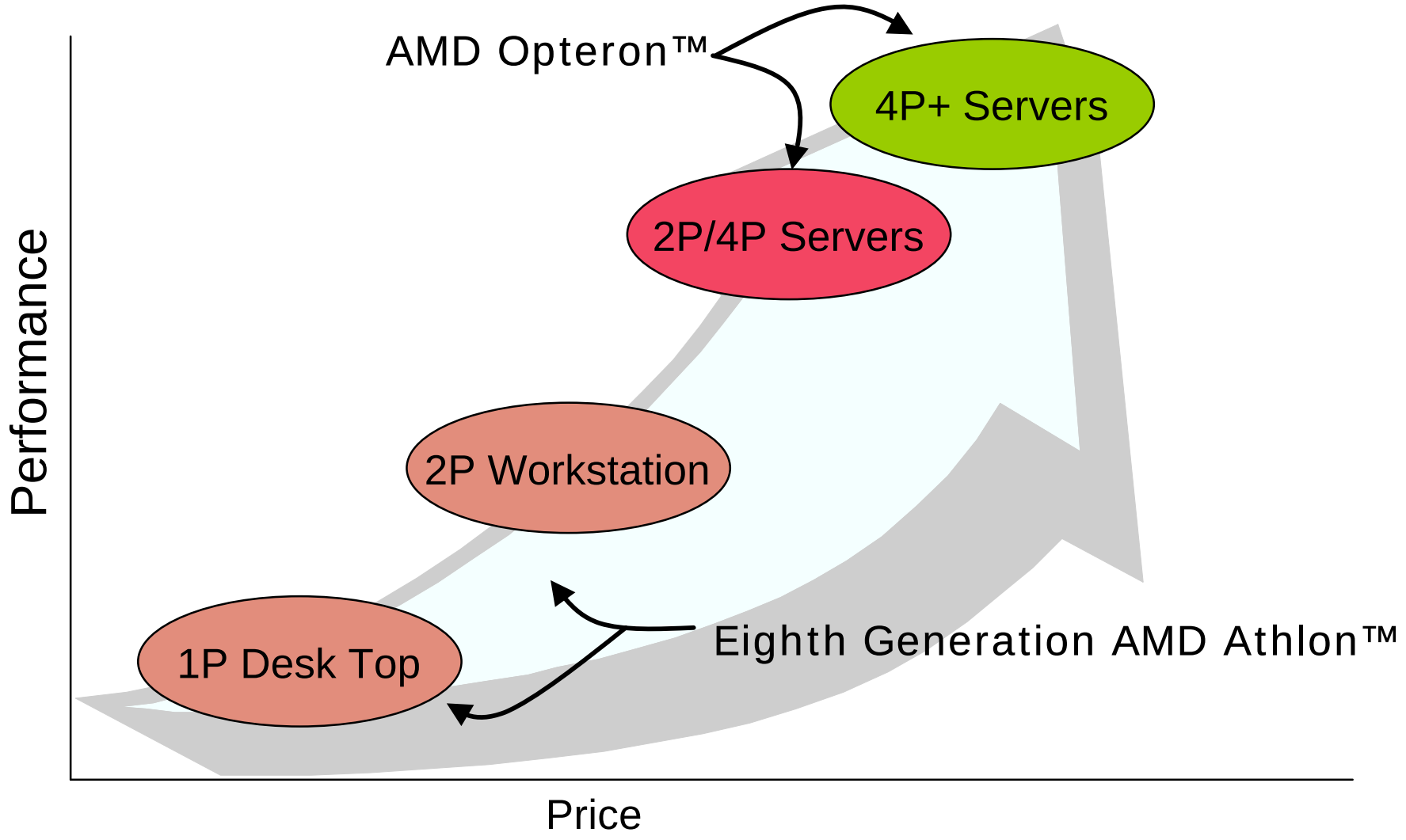
Eighth Generation AMD Athlon™ Based System



System Strengths

- Memory Latency, Bandwidth and memory reach:
  - 2^{40} physical (1 Terabyte)
  - 2^{48} virtual
- I/O Latency and Bandwidth ~1600M T/sec
- Glueless multiprocessing
- 64-bit CPU with large L2 Cache
- More Reliable – chip count

A Family of x86-64 Processors



Goal for AMD Eighth Generation Processor Family

- Build a next generation system architecture which serves as the foundation for future processor platforms

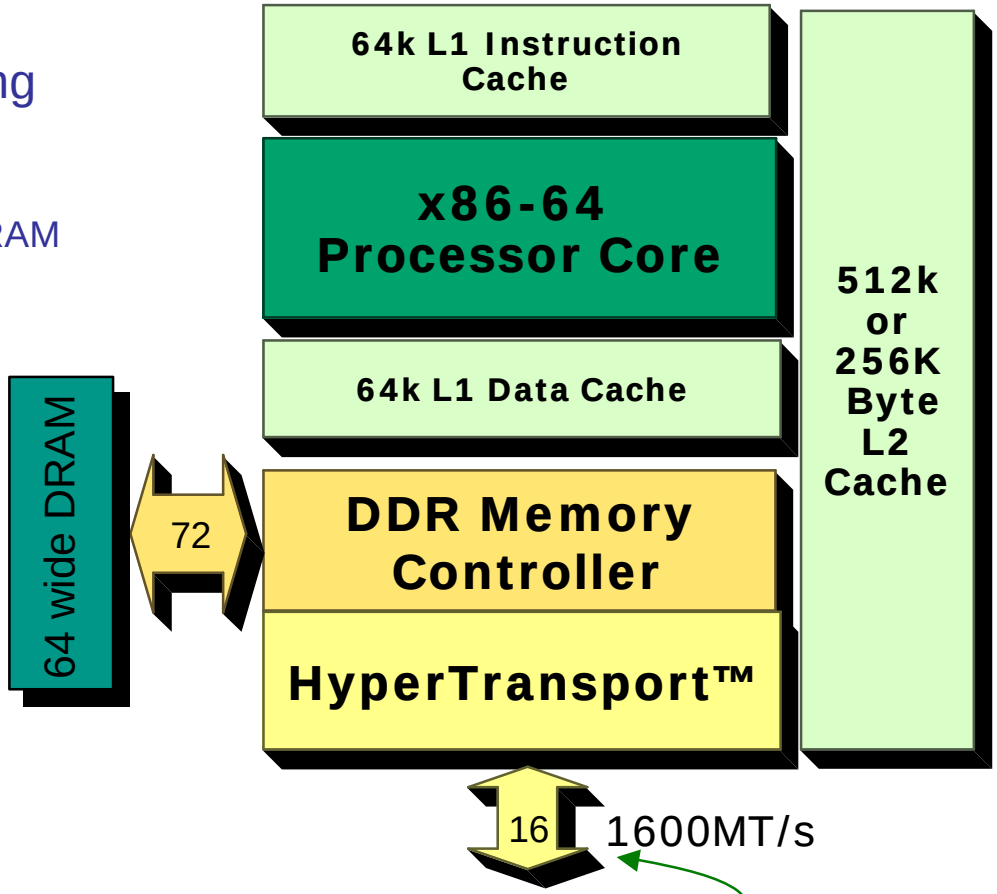
- Enable a full line of server and workstation products
  - Leading edge x86 (32- bit) performance and compatibility
  - Native 64- bit support
  - Establish, Promote and Execute on an industry standard x86-64 Instruction Set Architecture
  - Glue less *Plug & Play* Multiprocessor support

- Provide top-to-bottom desktop and mobile processors

Eighth Generation AMD Athlon™ Processor:

❑ Desktop Processor

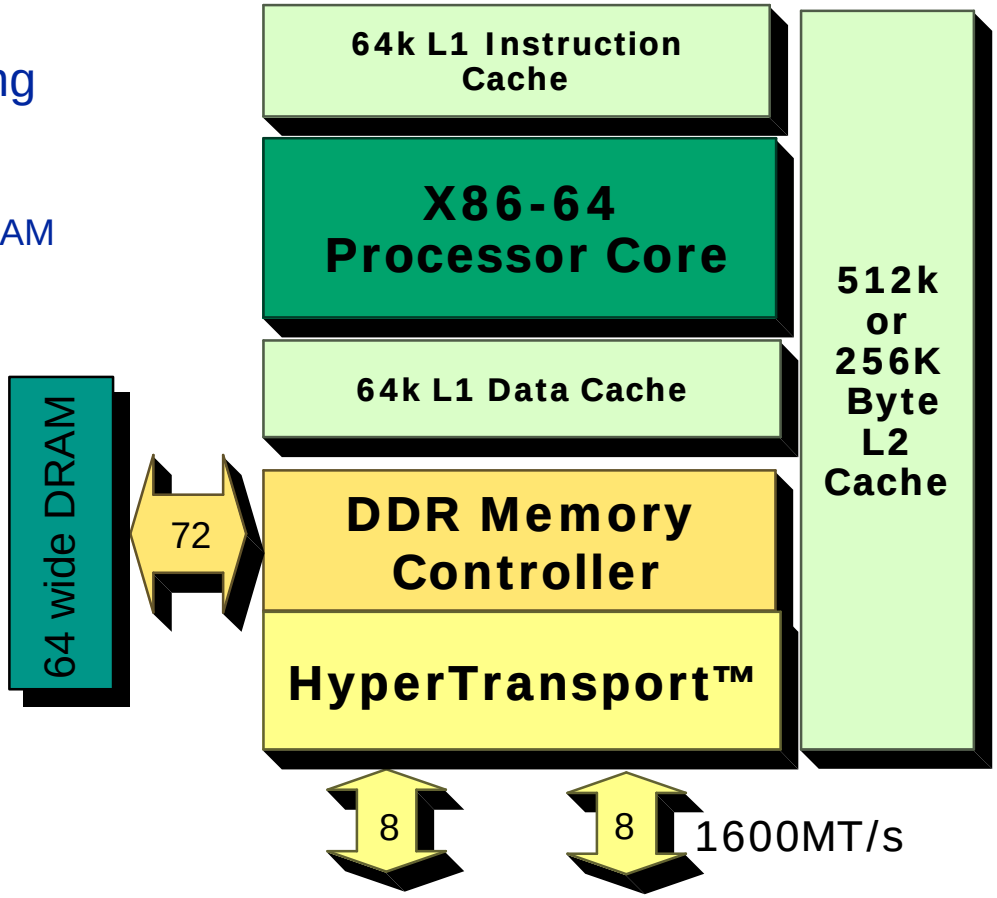
- X86-64 bit 1P Desktop Processor
- One 72-bit DDR channel supporting *200, 266*, and *333* MHz
  - ✓ Supports Up to 4GB of local DDR DRAM
  - ✓ Future memory technology supported
- One 16-bit HyperTransport Link
- On chip L1 & L2 cache
  - ✓ 64K-Byte L1 Inst.
  - ✓ 64K-Byte L1 DATA
  - ✓ 256/512KB ECC protected L2
- 754-pin mPGA Package



Eighth Generation AMD Athlon™ Processor:

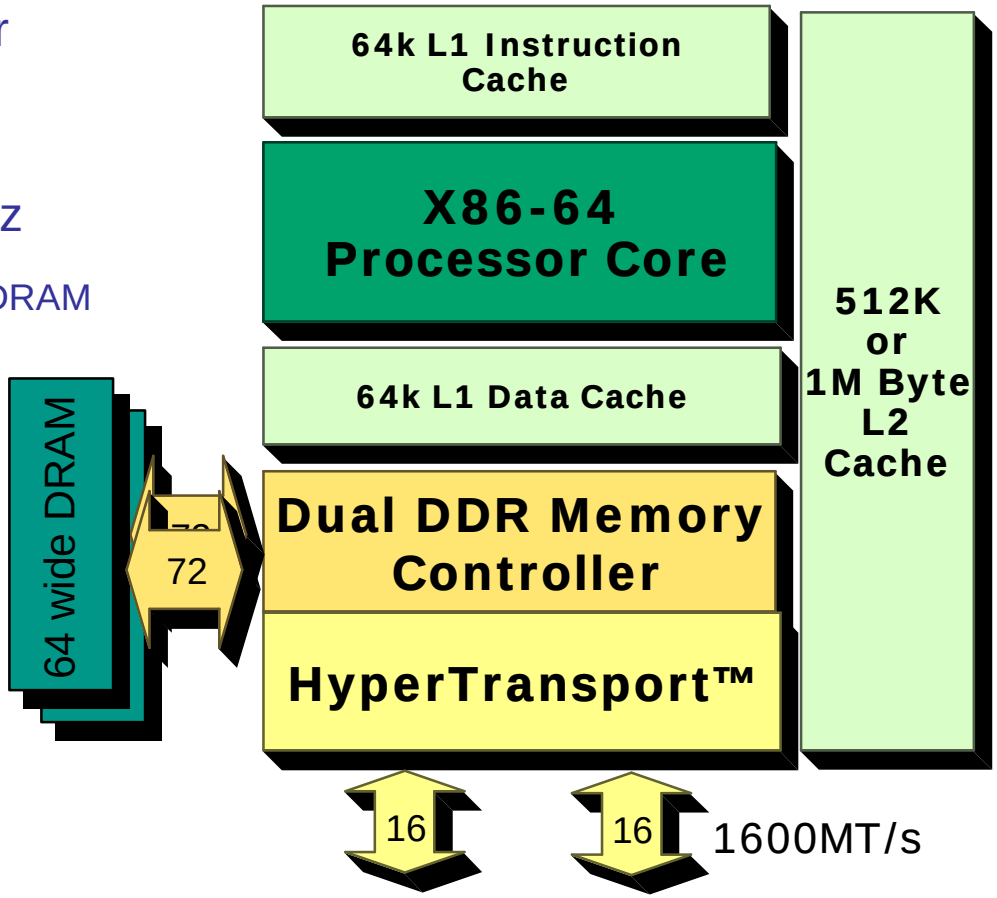
❑ Desktop Processor

- X86-64 bit **2P** Desktop Processor
- One 72-bit DDR channel supporting *200, 266*, and *333* MHz
  - ✓ Supports Up to 4GB of local DDR DRAM
  - ✓ Future memory technology supported
- **Or two 8-bit** HTT Links
- On chip L1 & L2 cache
  - ✓ 64K-Byte L1 Inst.
  - ✓ 64K-Byte L1 DATA
  - ✓ 256/512KB ECC protected L2
- 754-pin mPGA Package



AMD Opteron™ Family Processors

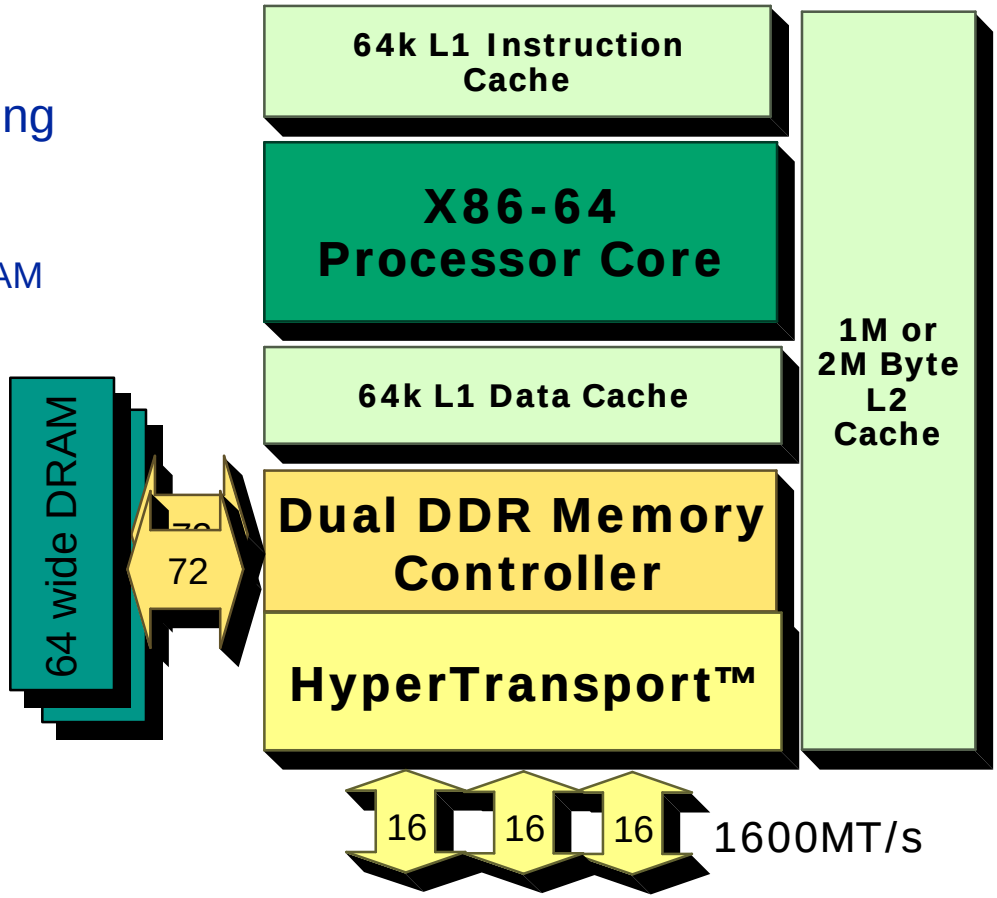
- **High end Workstation**
  - 64-bit 2P Server-Class Processor
  - Two 72-bit DDR channels supporting 200, 266, and 333 MHz
    - ✓ Supports Up to 8GB of local DDR DRAM
    - ✓ Future memory technology support
  - 2 16-bit HTT Links
  - Larger on chip L2 cache
    - ✓ 64K-Byte L1 Inst.
    - ✓ 64K-Byte L1 DATA
    - ✓ 512/1024KB ECC protected L2
  - 940-pin mPGA Package



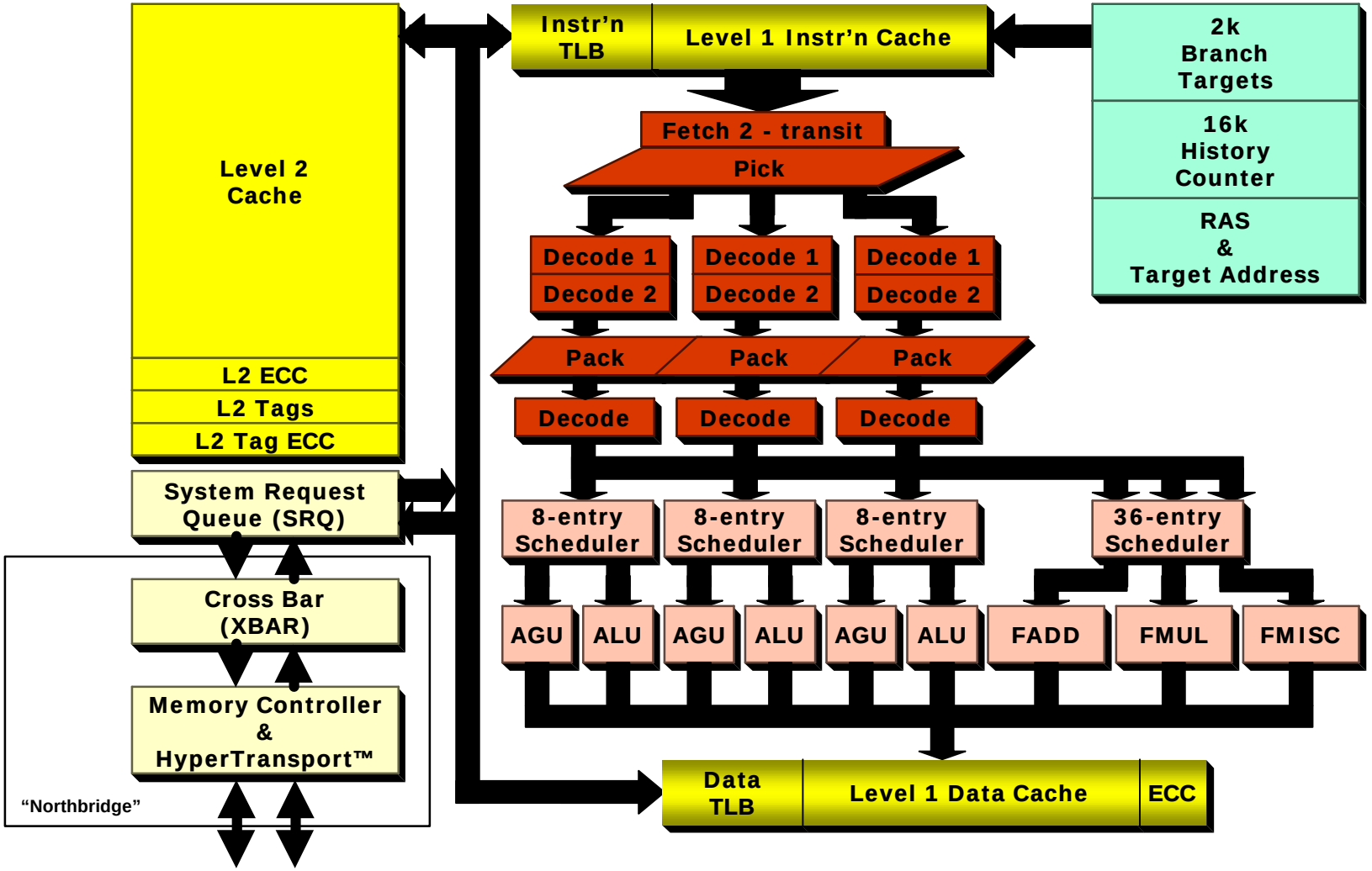
AMD Opteron™ Family Processors

❑ High end Server

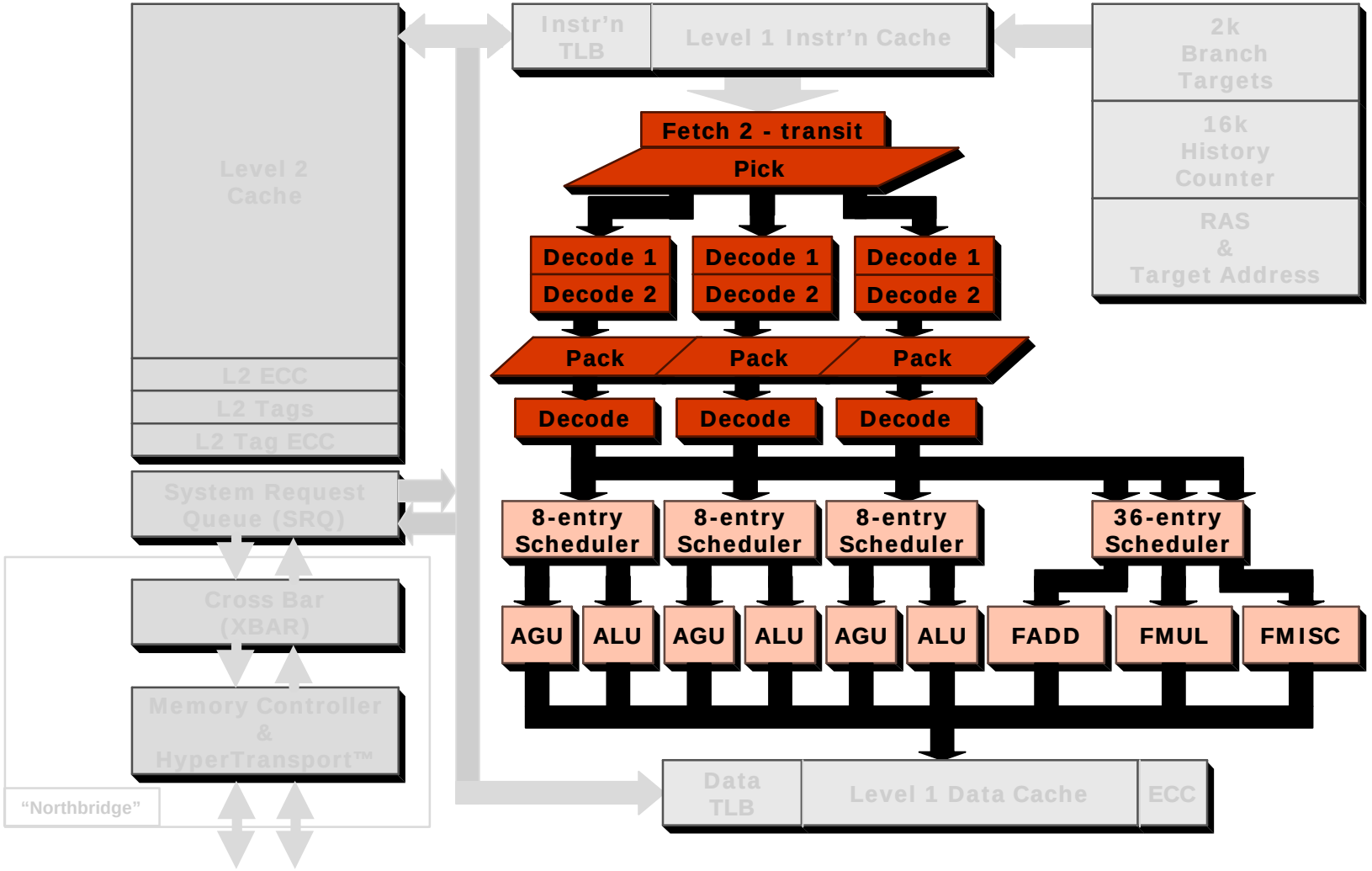
- 64-bit 8P Server-Class Processor
- Two 72-bit DDR channels supporting 200, 266, and 333 MHz
  - ✓ Supports Up to 8GB of local DDR DRAM
  - ✓ Future memory technology support
- *3* 16-bit HyperTransport Links
- Still Larger on chip L2 cache
  - ✓ 64K-Byte L1 Inst.
  - ✓ 64K-Byte L1 DATA
  - ✓ 1M/2MB ECC protected L2
- 940-pin mPGA Package



The four elements of AMD Opteron™ and Eighth Gen. AMD Athlon™



The x86-64 CPU



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x86-64 vs. x86-32 Register Differences

❑x86-64

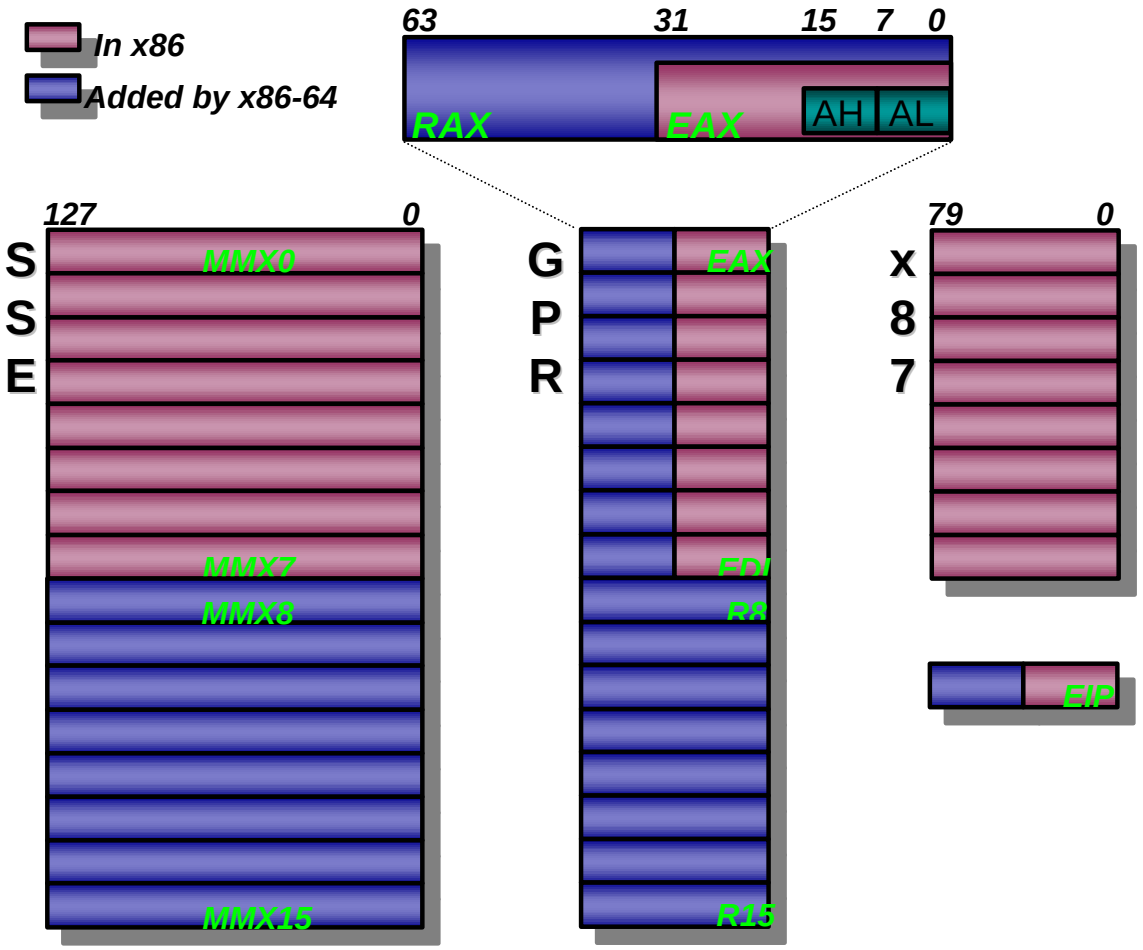
- ➢ 64-bit integer registers
- ➢ 48-bit Virtual Address
- ➢ 40-bit Physical Address

❑REX - Register Extensions

- ➢ Sixteen 64-bit integer registers
- ➢ Sixteen 128-bit SSE registers

❑SSE2 Instruction Set

- ➢ New
  - ▪ Double precision scalar and vector operations
  - ▪ 16*8, 8*16 way vector MMX operations
- ➢ SSE1 already added with AMD Athlon XP



Computing Strategy: x86-64

Legacy: 32-bit Mode

- Both AMD Athlon™ and AMD Opteron™ run any 32-bit legacy O/S
- Compatible all legacy Drivers, OS & BIOS
- No application recompile required, no emulation layer

64-bit Mode

- Desired applications can be written/ported to leverage the full 64-bit capabilities of x86-64
  - Migrate only where warranted, and at the user's pace
- All 32-bit applications run under 64-bit OS
- BIOS is standard x86 32-bit code.
  - Transfer to 64-bit operation occurs under OS load/startup control

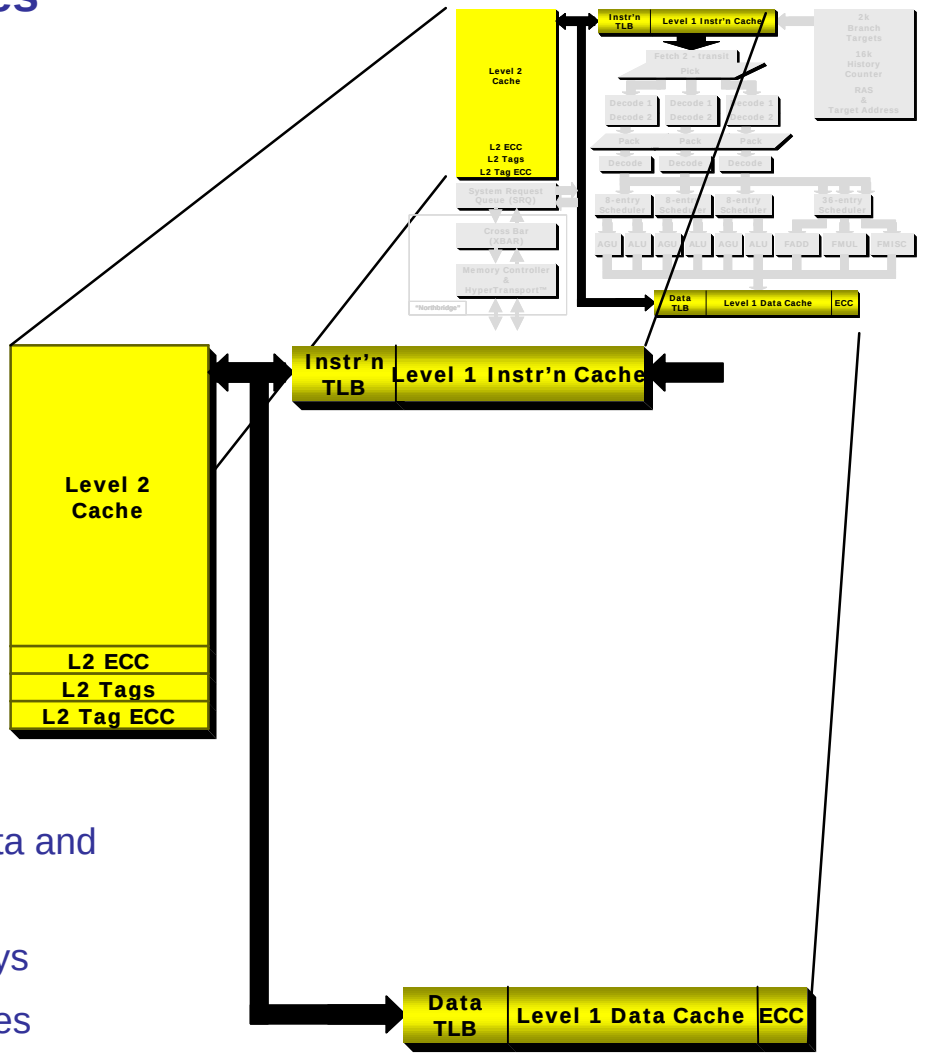
Other Core Performance Features

- 24-entry integer scheduler (vs. 18-entry on AMD Athlon XP)
- Improved instruction packing
- Miscellaneous instruction speedups
- Faster integer multiplies
  - Excellent Floating Point Processor for DSP applications

Multiply Latencies	8-bit, 16-bit	32-bit	64-bit
Athlon™ XP	3 cycles	4 cycles	N/A
Eighth Gen. Athlon™	3 cycles	3 cycles	4 cycles

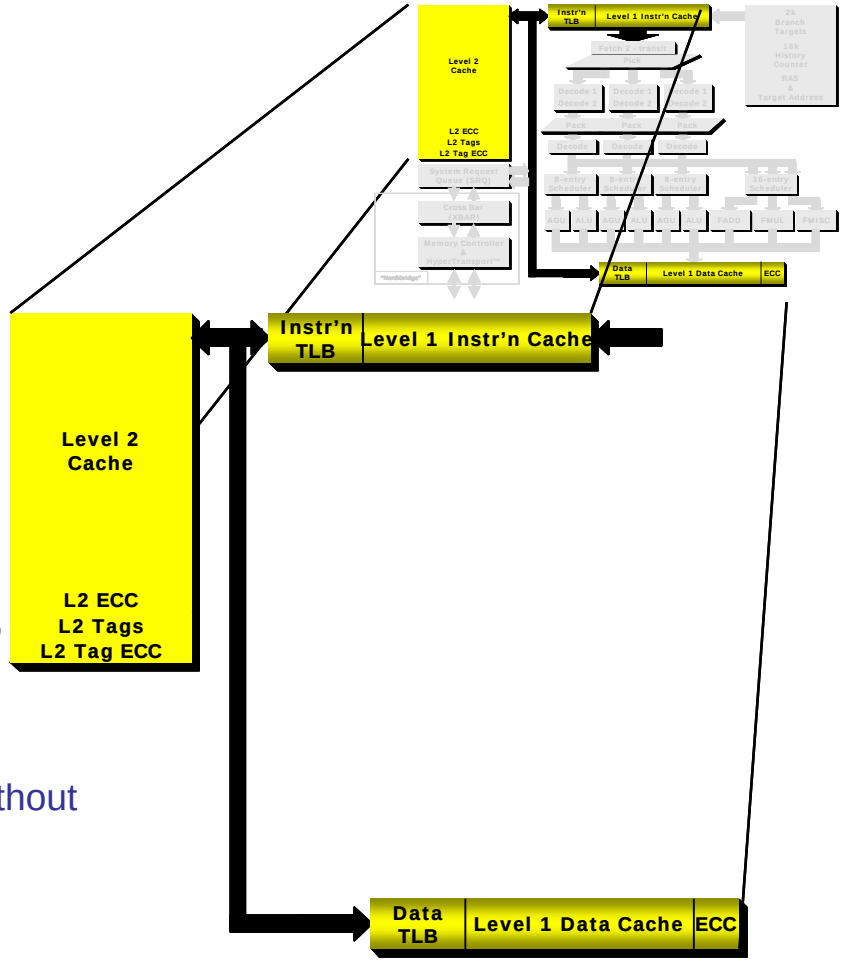
Internal Caching

- **64K-Byte 2-way associative L1 caches**
  - 64K-Byte ECC protected L1 D-Cache
  - 64K-Byte Parity protected L1 I-Cache
- **256K-Byte/512K-Byte/1M-Byte ECC protected L2 cache**
  - 16-way associative
  - Improved L2 -> L1 bandwidth (>2X Athlon)
  - L2 backs up branch prediction and pre-decode information and data
- **Enhanced reliability**
  - ECC protected L1 data cache, L2 tags and data and DRAM
  - Hardware scrubbing of all ECC protected arrays
  - Machine check architecture for reporting failures



Internal TLB Cache

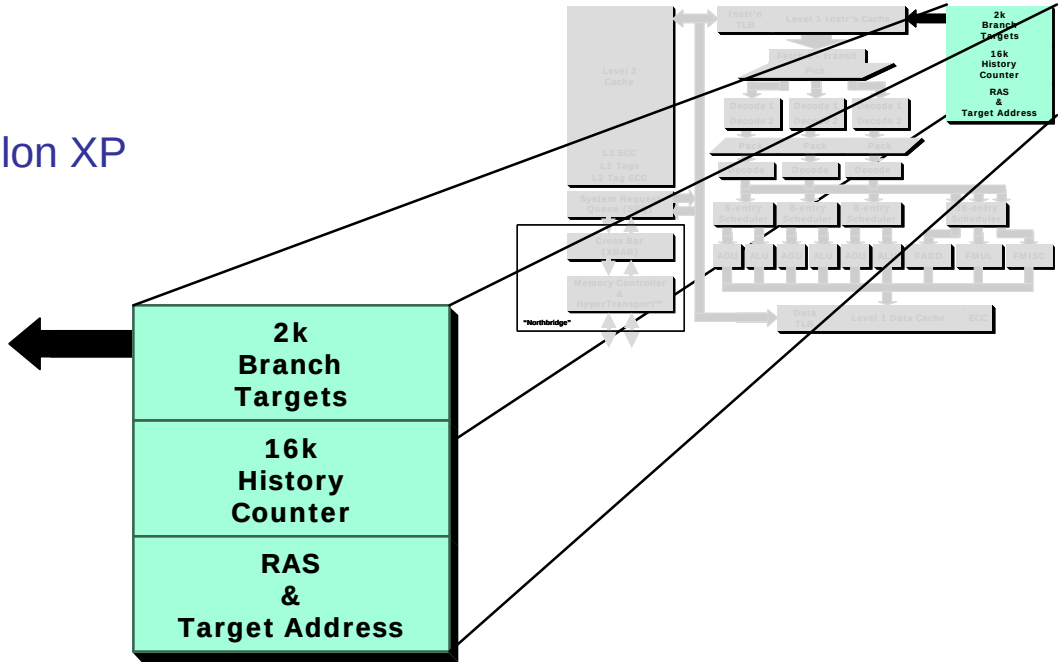
- **Translation Look-aside Buffer (TLB) for large Multiprocessor workloads**
  - 512 entry L2 TLB and Data TLB (4-way associative)
    - Twice the size as AMD Athlon XP
  - 32 entry L1 Instruction TLB (4K Pages - fully associative)
    - Twice the size as Athlon™ XP
    - Same 32 entry DTLB (4K Pages) and 8 entry ITLB/DTLB (2M/4M pages)
  - Lower latencies then AMD Athlon XP
  - TLB flush filter
    - Allows multiple processes to share TLB without SW intervention
    - HW snooping of page tables



Branch Prediction

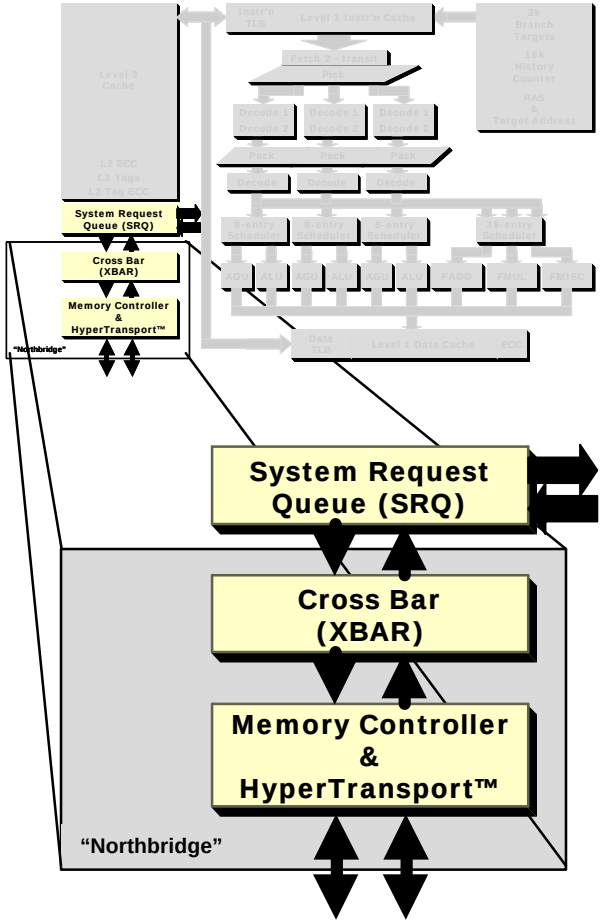
❑ Branch Prediction

- ➢ Full L1 Cache Coverage
  - Twice the selectors as AMD Athlon XP
- ➢ 2K Branch Target Addresses
  - Same size as AMD Athlon XP
  - Backed up by Branch Address Calculator
  - Early correction (5 cycle) of miss-predict
- ➢ 16K Bimodal Counters
  - Four times AMD Athlon XP
- ➢ Full Pre-decode and Branch Identification in L2 Cache
  - New and unique to Eighth Generation Family of Processors
  - Reuses L2 ECC bits on clean/shared instruction lines and on extra bit

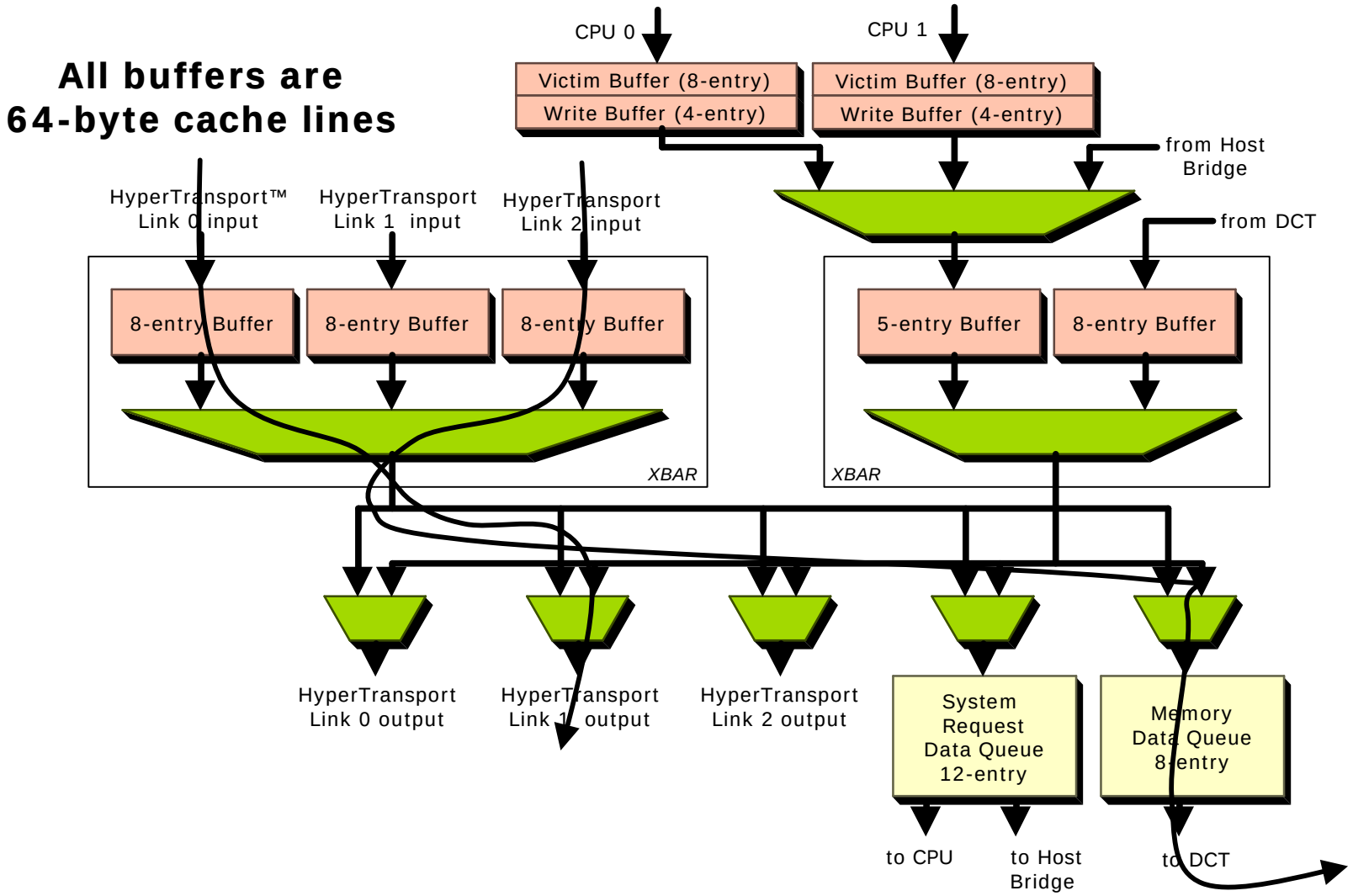


Integrated Northbridge

- **Performs same functions found in Northbridge**
  - Memory Controller
  - Host-Bridge function as defined by the PCI spec
  - PCI-to-PCI Bridge as defined by the PCI spec
  - Graphics Address Resolution Table (GART)
  - Multi-processor coherency
- **Controlled via PCI configuration registers**
  - Not related to CPU(s) on the same die
  - Memory controller configuration
  - HyperTransport routing
- **Configured by Firmware**
  - HyperTransport initialization via Hardware
    - Auto-size, coherent or not, “Legacy” path to the ROM in Southbridge
  - HyperTransport speed and routing via firmware
  - Everything else in firmware follows existing paradigms
    - PCI enumeration
    - Memory sizing and configuration
    - I/O controller setup

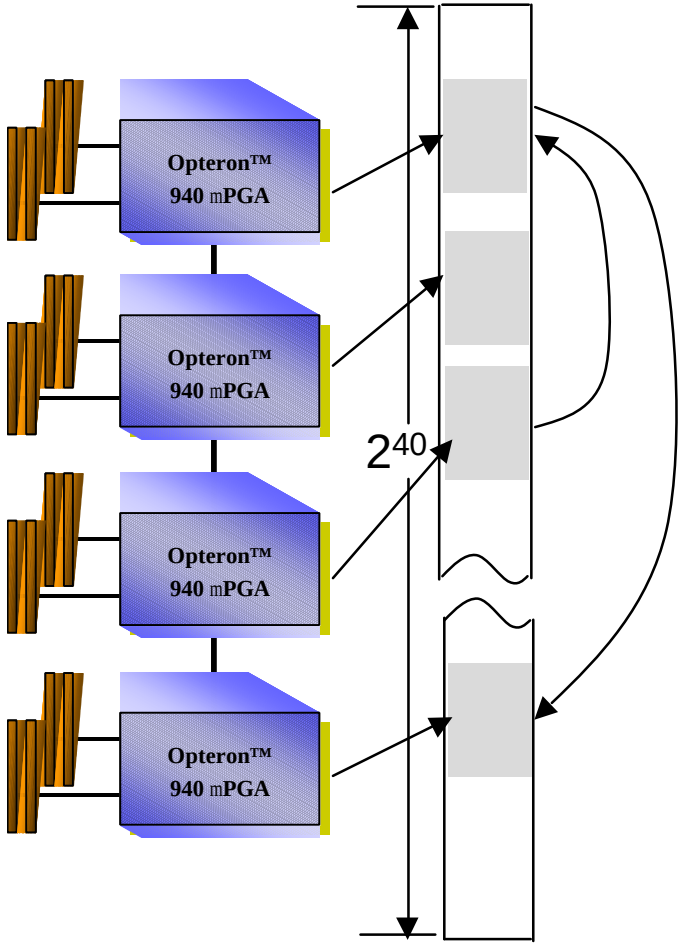


Northbridge Data Flow



Processors with multiple HyperTransport™ interfaces

- Data movement over the HyperTransport™ bus does not use any CPU machine cycles.
- External device can write to any address within the Processor's physical 40-bit address range without CPU intervention.
- In cases where there are multiple HyperTransport™ ports, data can be passed between ports without CPU intervention.
- Because all devices reside within one physical 2^{40} linear space all I/O devices have access to all processors and their associated memory & I/O.



Advantages of Integrated DDR DRAM Controller

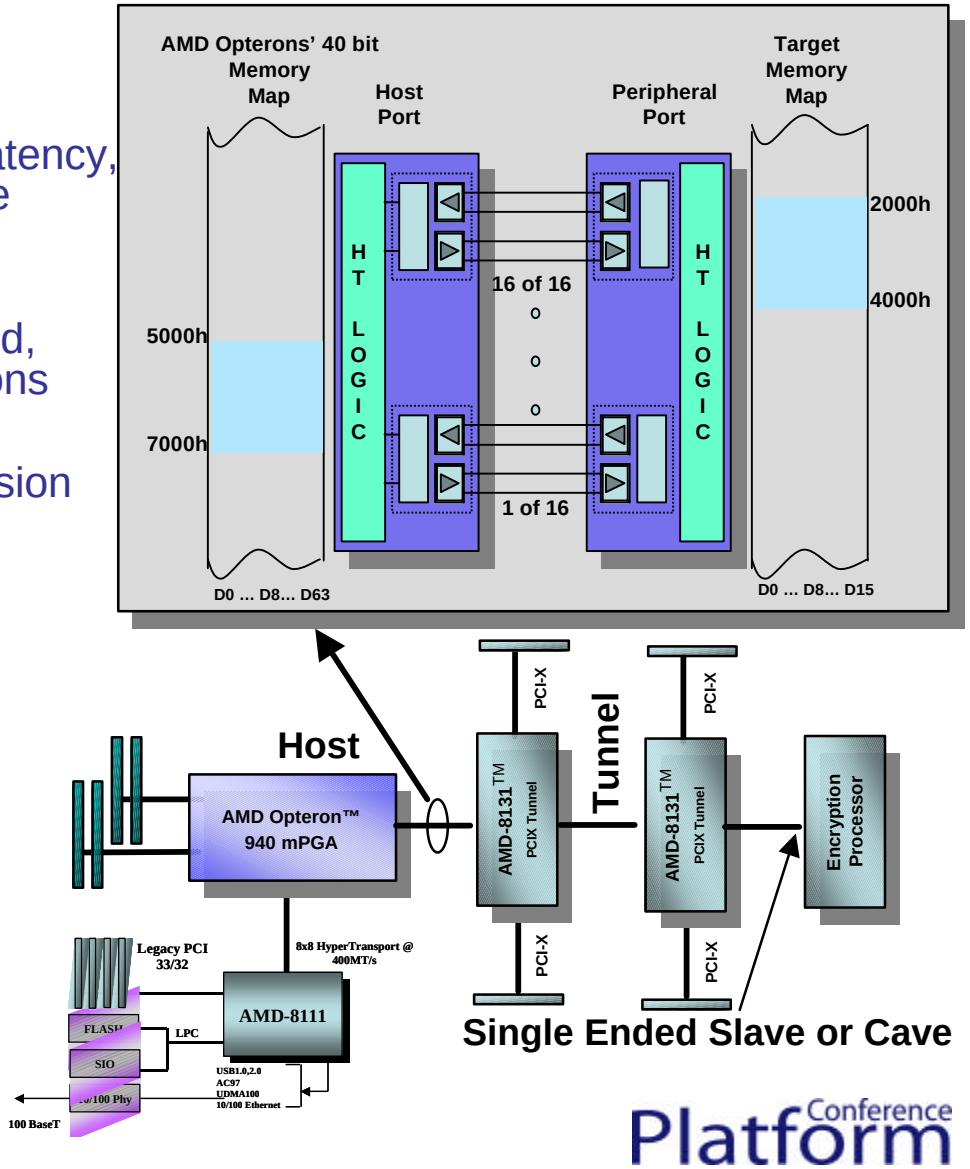
- Reduced Latency to Memory
  - No need to traverse a front side bus
  - Northbridge runs at CPU speed
- Higher bandwidth between memory controller and CPU
  - The path between Northbridge and CPU is 8 bytes wide and runs at processor speed
- Memory bandwidth scales with processor count
  - When you add a processor, you add a memory controller
- Performance tuning registers for the memory controller are accessible at user level during run time
  - Monitor contiguous memory hits / misses, L2 efficiency,…

AMD's commitment to next Gen DDR

- **DDR200,266,333 supported at launch**
  - AMD is actively involved with the development community (JEDEC) in engineering the standard for DDR333
  - AMD expects the AMD Opteron class of processors to ship with DDR333 support
  - AMD committed to leading the industry in open-standard DRAM evolution beyond DDR333

System I/O – HyperTransport™

- All processor HyperTransport Host Ports can be configured as either:
  - Coherent (SUMO architectures)
  - Non-coherent (simple I/O)
- Can be viewed as a high performance, low latency, Point-to-point transmission path between the processor and attached peripheral
- Transactions over the interface can be viewed, at the system level, as PCI-to-PCI transactions
- Enumeration of attached devices is an extension of PCI enumeration SW
- Address are routed within global 40 bit memory mapped address range per chain
- Up to 31 host/slave devices can be attached to any one HyperTransport Host port
- Arbitration, Ordering & CRC error checking
- Support for 2, 4, 8, 16 bit widths from 200MHz to 800MHz DDR



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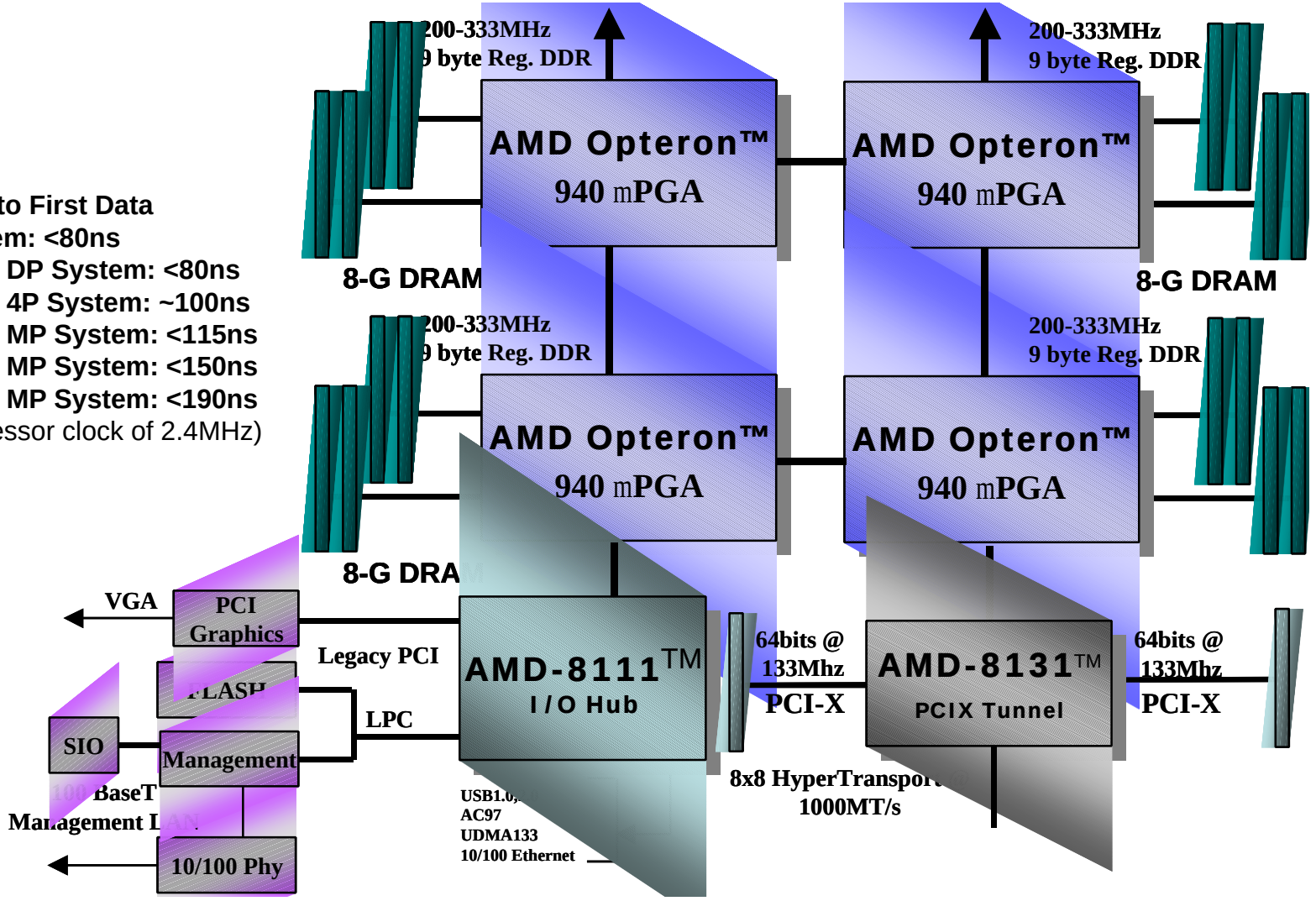
Multiprocessing with AMD Opteron™

- **Non Uniform Memory Architectures (NUMA)**
  - Brings dramatic scalable advantages
  - Software management is difficult
- **Symmetric Multi Processing (SMP)**
  - Topology brings dramatically simplified software model
  - Memory system doesn't scale as processors are added
- **Sufficiently Uniform Memory Organization (SUMO)**
  - Does both:
    - Software view of memory is SMP
      - Physical address space is flat and fully coherent
      - Latency difference between local and remote memory in an 8P system is comparable to the difference between a DRAM page hit and DRAM page conflict
      - DRAM can be contiguous or interleaved
  - Additional processor nodes bring true increased memory bandwidth
- **Multiprocessor support inherent in design (not an add on)**
  - Lower overall system chip count (glue-less interface)

AMD Opteron™ Glue-less SUMO Multiprocessing

- Idle Latencies to First Data
  - 1P System: <80ns
  - 0-Hop in DP System: <80ns
  - 0-Hop in 4P System: ~100ns
  - 1-Hop in MP System: <115ns
  - 2-Hop in MP System: <150ns
  - 3-Hop in MP System: <190ns

(Assume a processor clock of 2.4MHz)



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The Rewards of Good Plumbing

➢ HyperTransport™ I/O Bandwidth

- 4P system designed to achieve *8GB/s aggregate memory copy bandwidth*
  - With data spread throughout system
- Current State of Art bus based systems limited to about 2.5GB/s aggregate bandwidth (3.2GB/s theoretical peak)

➢ Latency

- Average unloaded latency in 4P system (page miss) is designed to be 140ns
- Average unloaded latency in 8P system (page miss) is designed to be 160ns
- Latency under load planned to increase much more slowly than bus based systems due to redundant data paths and available bandwidth
- Latency shrinks quickly with increasing CPU clock speed and HyperTransport link speed

Eighth Generation Processor Family Summary

- **Optimized for high frequency operation**
  - Chip infrastructure optimized for sub 0.10m process impacting:
    - Power distribution
    - Clocking
    - Circuit design and layout
  - Pipeline increased 2 cycles over AMD Athlon XP
    - 10 to 12 cycles for integer pipeline
    - optimize for frequency and Inter-Processor Communications (IPC)
- **20-25% better performance than AMD Athlon XP**
  - Smart low-latency memory controller
  - Advanced clock distribution methods
- **Integrated Next Generation Intelligent cache**
  - L1 Data Cache Translation Look-aside Buffers (TLB) improvements
  - Branch prediction
- **Integrated DDR Memory System Controller**
  - Closing the gap between external memory access and CPU speed
  - <1/2 latency of current Stare of Art (AMD Athlon XP processor)
  - >4X the bandwidth of current State of Art (AMD Athlon XP system)
- **Integrated HyperTransport™ I/O supporting**
  - High speed peripheral connections - >3.2GB throughput (>6.4GB full duplex)
  - Coherent HyperTransport™ Technology to support glue-less MP interface

Platform Conference

AMD Opteron™ and AMD Athlon™ Applications

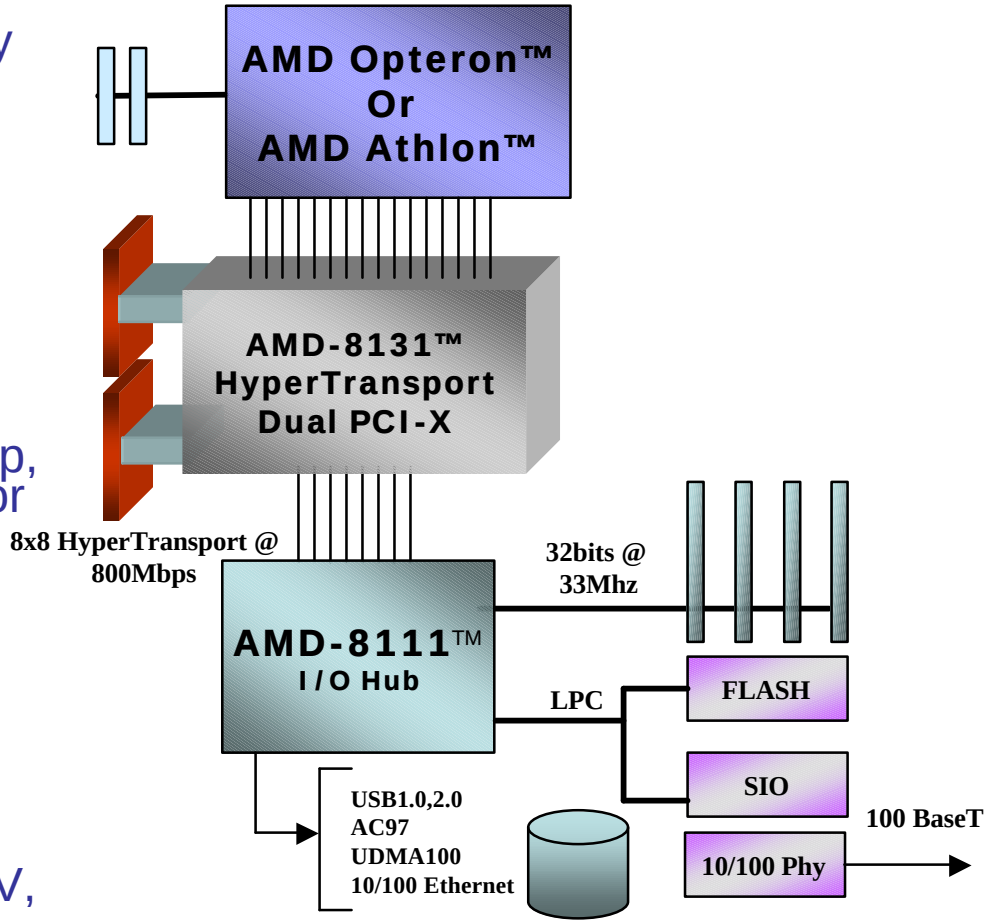
AMD Opteron™ Support IC's

- AMD is committed to deliver the highest quality systems solutions
- Providing a family of x86-64 processors is just the start
- AMD will promote and enable a broad range of HyperTransport™ support silicon from internal and external design efforts.
- AMD, with the HyperTransport consortium, will grow the HyperTransport eco-system

AMD-8131™ HyperTransport™ PCI-X Tunnel

❑Dual PCIx Master

- Each PCI-X Bridge independently supports
  - 66, 100, 133MHz PCI-X Protocol
  - 33 and 66MHz PCI 2.2 Protocol
  - SHPC Controller
  - 64-bit data path
  - IOAPIC
  - Arbiter for up to 5 masters
  - Hot-swap
- HyperTransport Support: 16/16 up, 8/8 down, independent support for
  - Up to 1600MT/s up and down
  - Full Link Auto sizing and speed selection
- 829 OBGA, 37.5mm body, 1.27mm pitch, full array, 6-Layer Motherboard Breakout
- Power Estimate: 4.4W: 1.2V, 1.8V, 3.3V Supplies

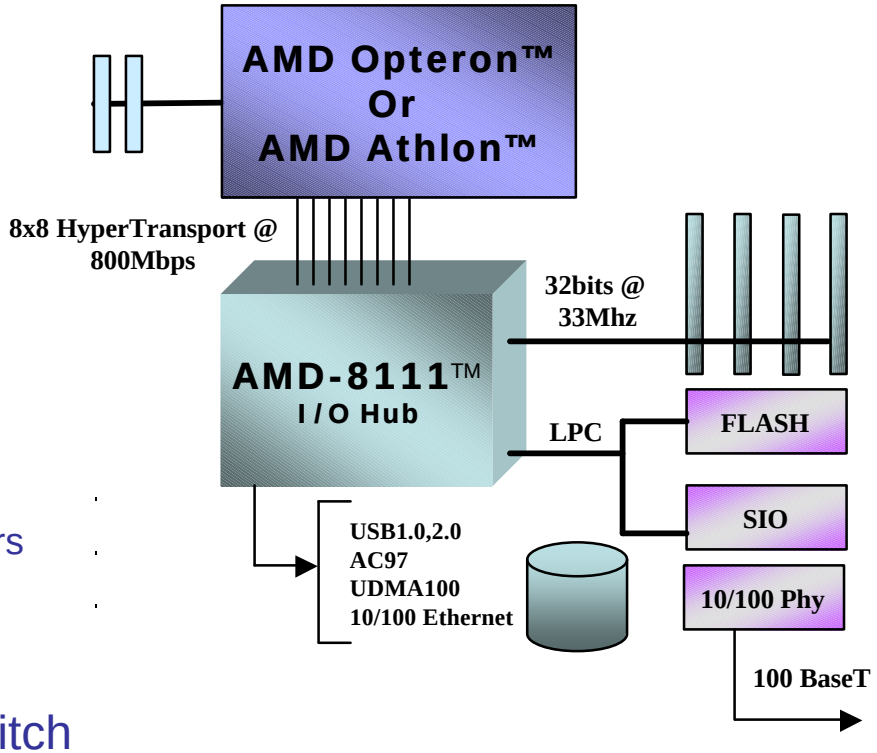


Platform Conference

AMD-8111™ HyperTransport™ I/O Hub

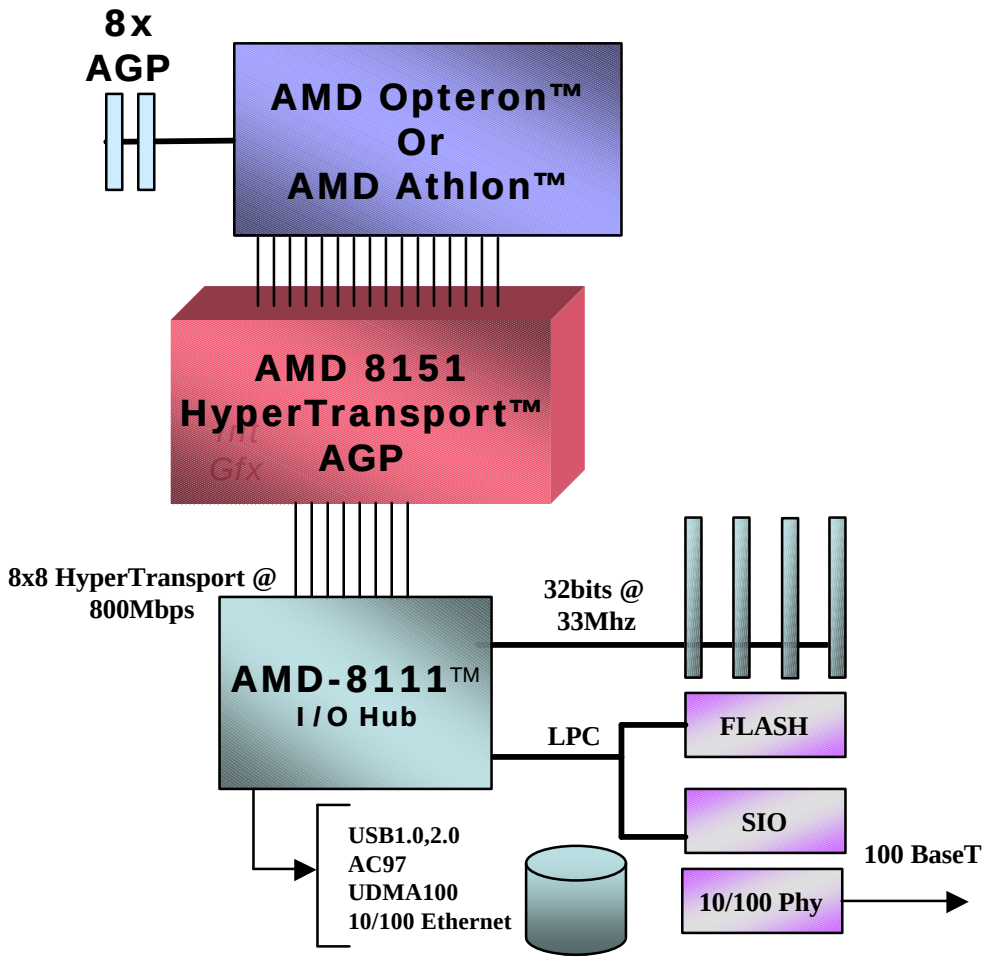
❑I/O Hub

- Engineered from past successful AMD I/O Hubs development efforts
- 8/8 wide 400 MHz HyperTransport interface (6.4 G bits/sec)
- Enhanced 10/100 Ethernet MAC
- USB1.0, USB2.0, UDMA133, AC'97
- LPC for ROM and SIO
- PCI 33/32 Bridge ("legacy")
  - Supports arbitration of up to 8 external masters
- SMbus 1.1 and 2.0 controllers
- 492 PBGA, 35x35mm body, 1.27mm pitch
- Power Estimate <2.0W: 1.2V, 1.8V, 3.3V Supplies

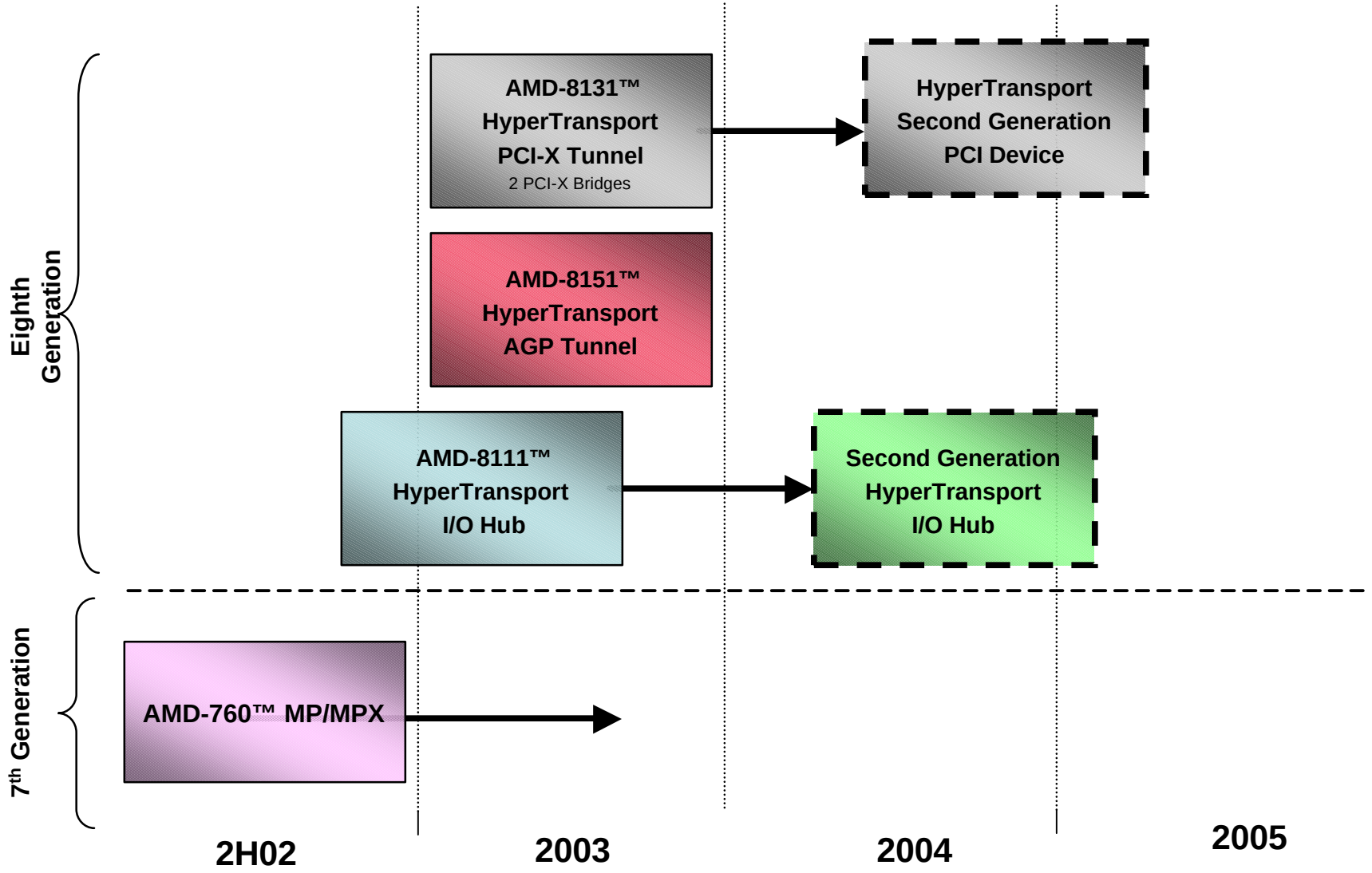


AMD-8151™ HyperTransport™ AGP Tunnel

- 8xAGP
  - Fully AGP 3.0 Compliant
  - 66,133,266,533MHz operation
- HyperTransport Support: 16/16 up, 8/8 down, independent support for
  - Up to 1600MT/s up, Up to 800MT/s down
  - Full Link Auto sizing and speed selection
- 564 OBGA, 31x31mm body, 1.27mm pitch, full array
- Power Estimate: 3.4W: 1.2V, 1.5V, 1.8V and 3.3V supplies



AMD Opteron™ & AMD Athlon™ Server Chipset Roadmap



A Growing ecosystem of HyperTransport™ enabled ICs

❑ Available today:

- Dual MIPS processor form Broadcom - BCM1250
- PCI 66/64 Bridge from SiPackets
- NITROX™ Security Macro Processor form Cavium Networks
- FPGA from XILINX and Altera

❑ Announced:

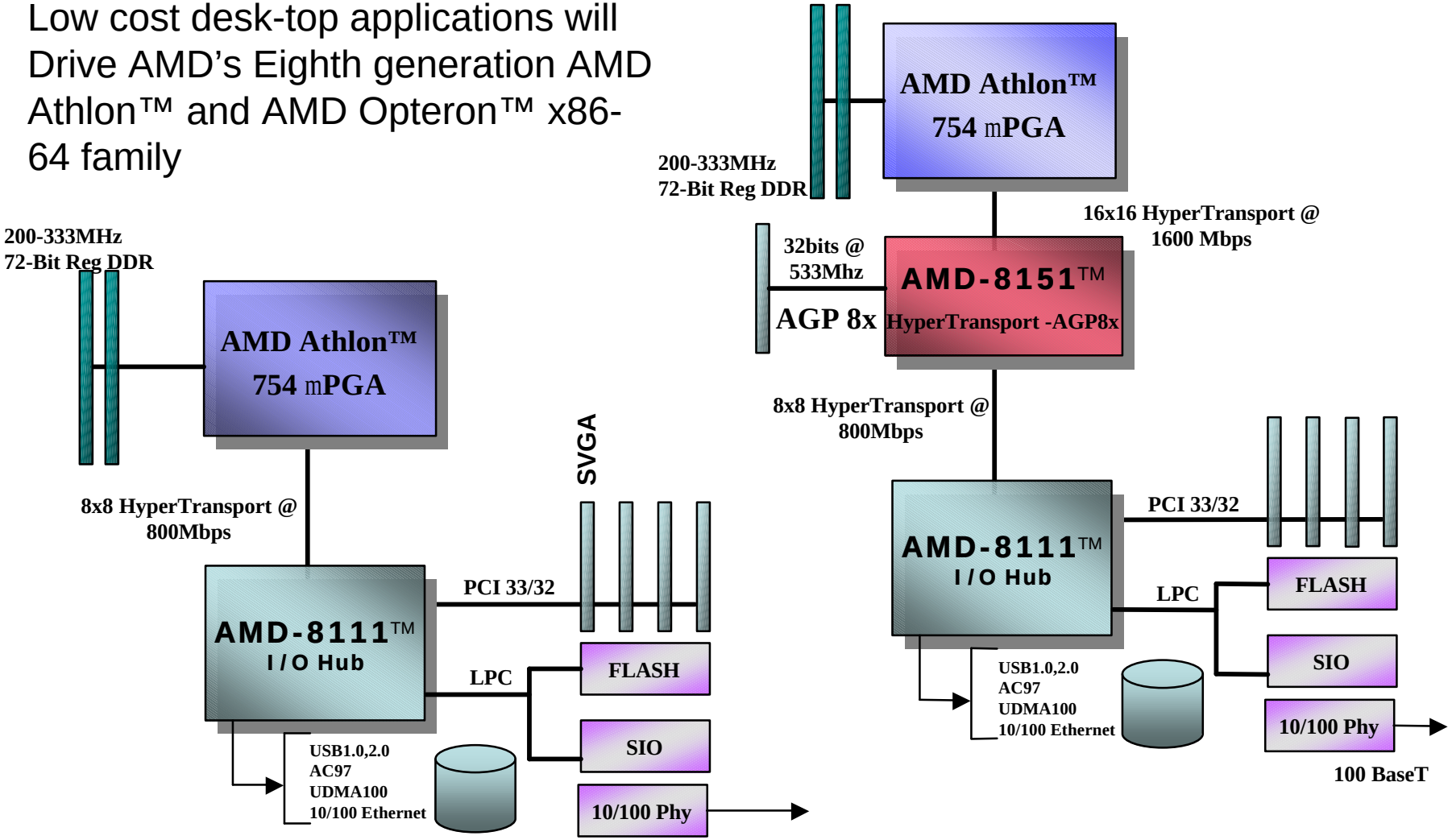
- RM9000 MIPS processor from PMC Sierra
- MIPS processor from SandCraft
- 4 Port 8/8 switch with hot-swap support from SiPackets
- SSL/IPsec packet processor with TCP/IP Offload – Hi/fn

❑ Planned:

- InfiniBand Bridge
- Fiberchannel Bridge
- StarFaberic Bridge/Tunnel
- Two new families of FPGA
- 4 port 16/16 Switches
- PCI-X Bridges
- Deep packet Processor
- Encryption/Packet classification

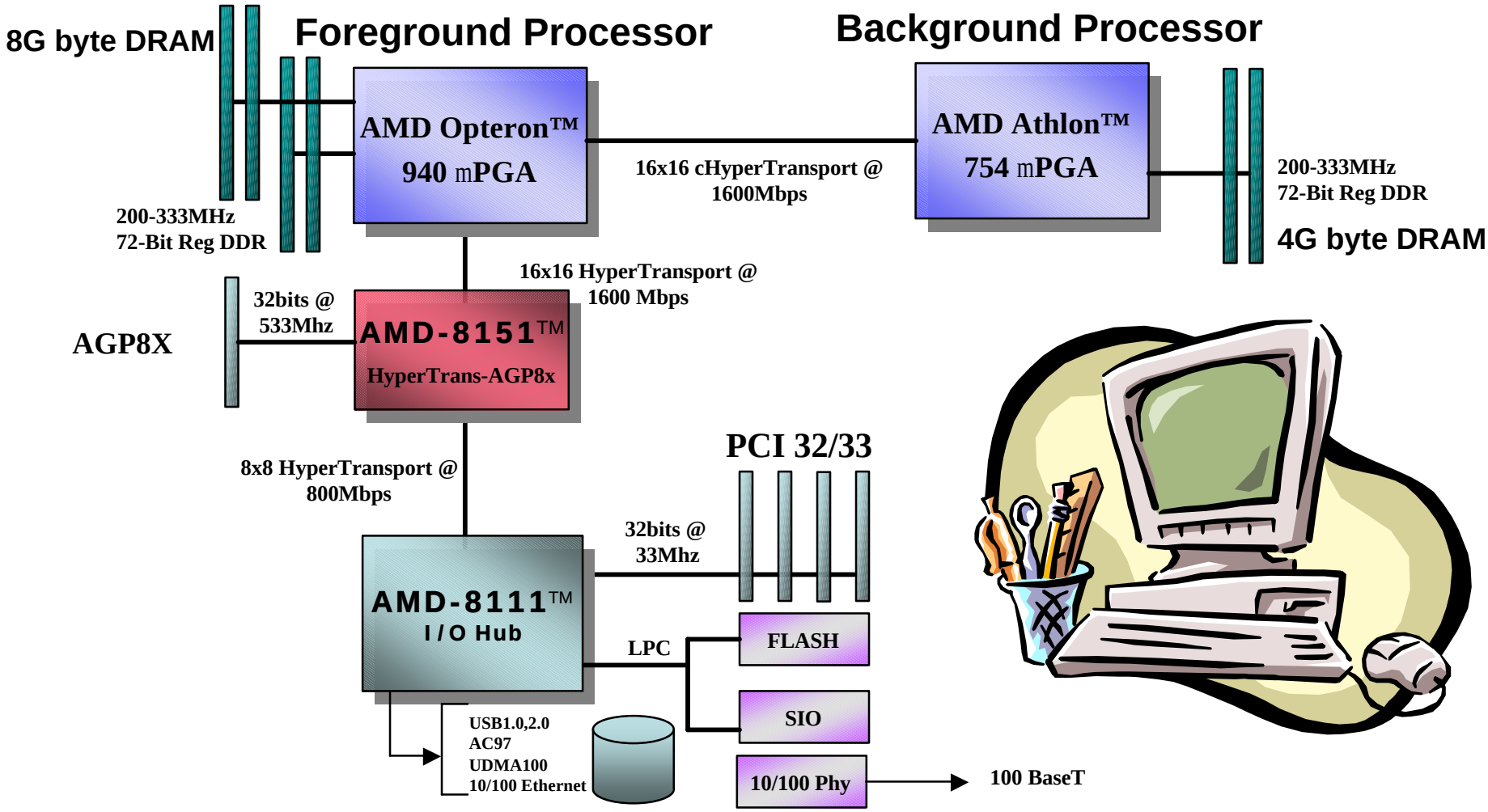
AMD Eighth Generation AMD Athlon™ Performance Desktop PC

Low cost desk-top applications will Drive AMD's Eighth generation AMD Athlon™ and AMD Opteron™ x86-64 family

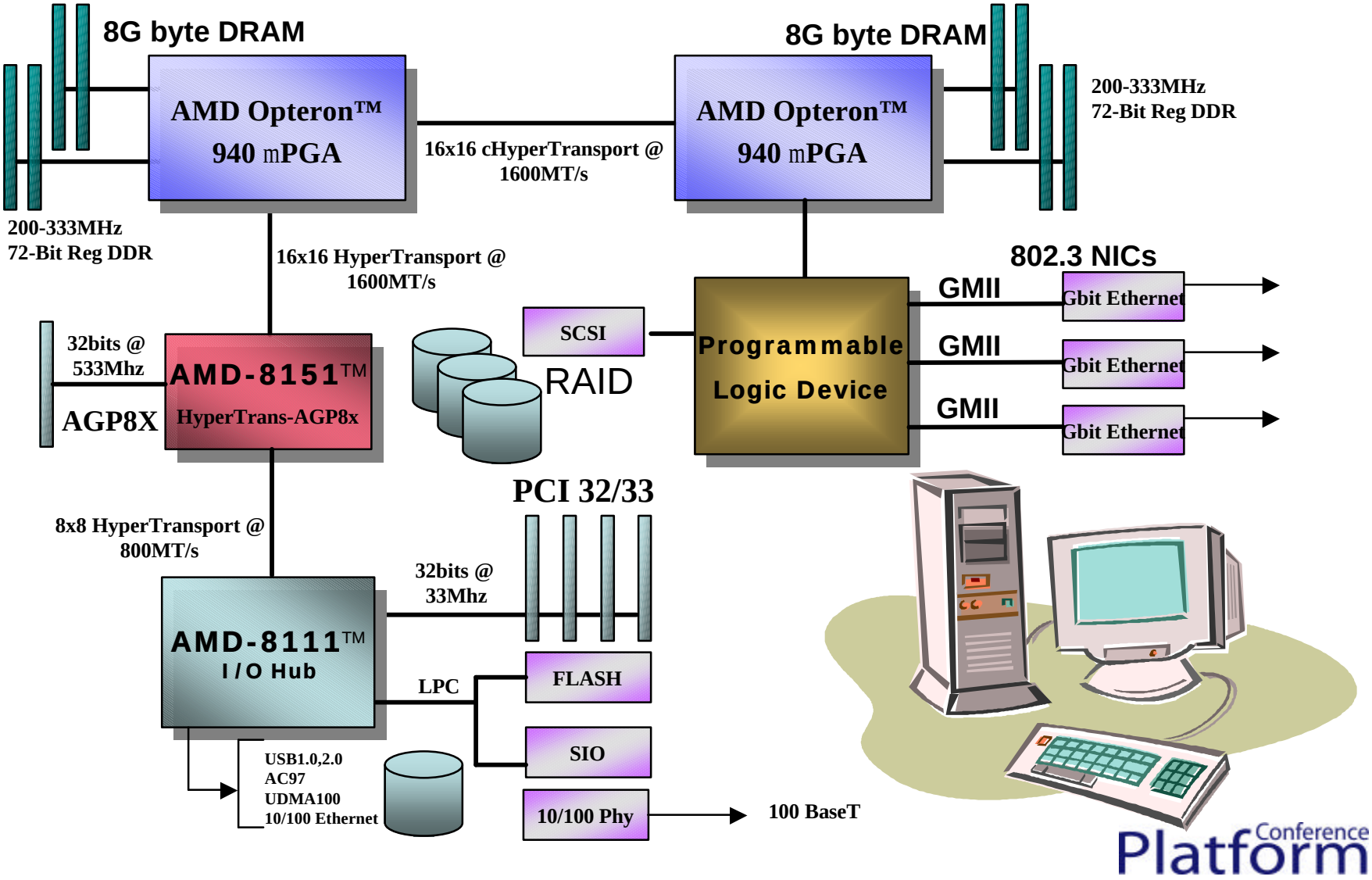


Platform Conference

AMD Opteron™ & AMD Athlon™ Asymmetric 2P Low Cost Desk-Top

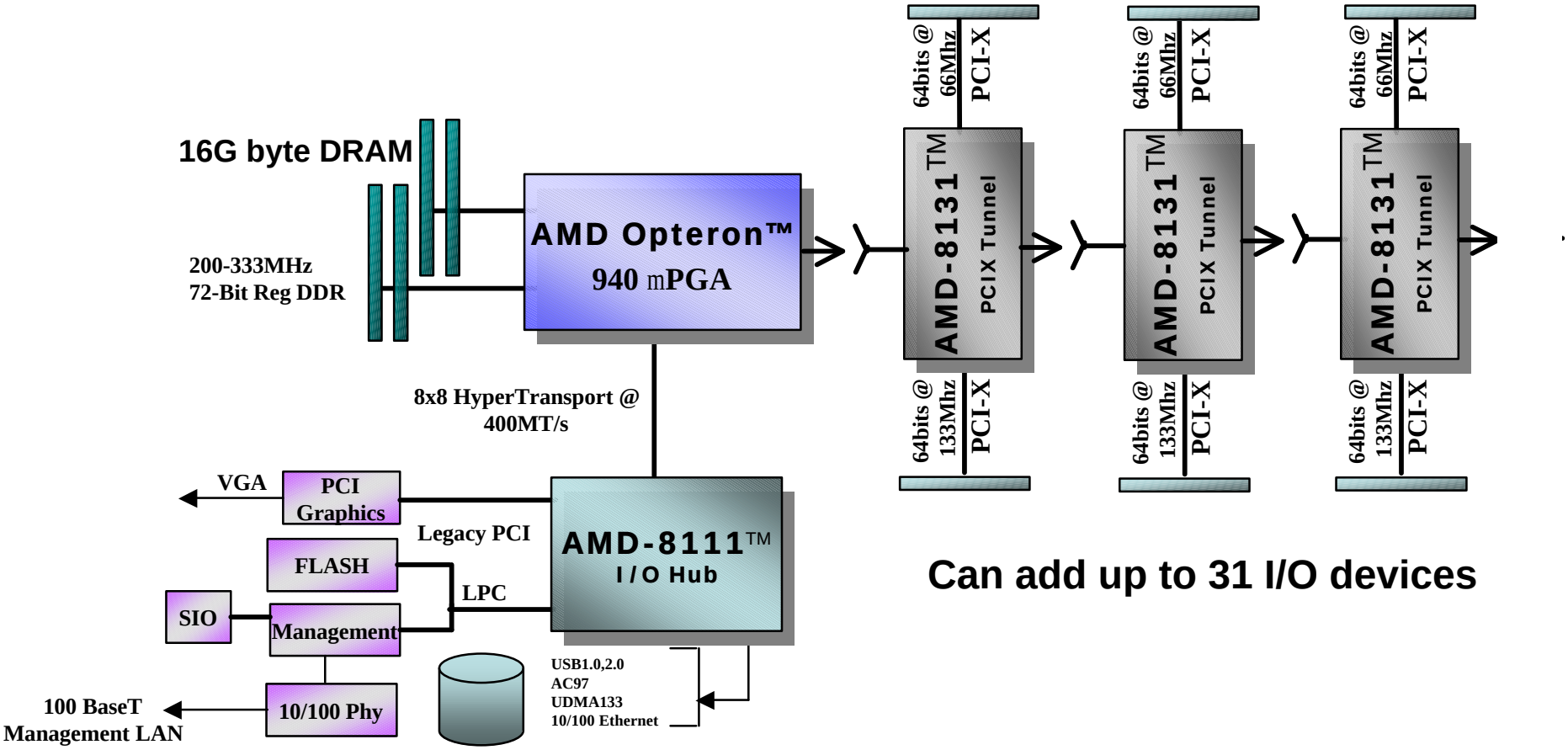


AMD Dual Opteron™ Symmetric Workstation



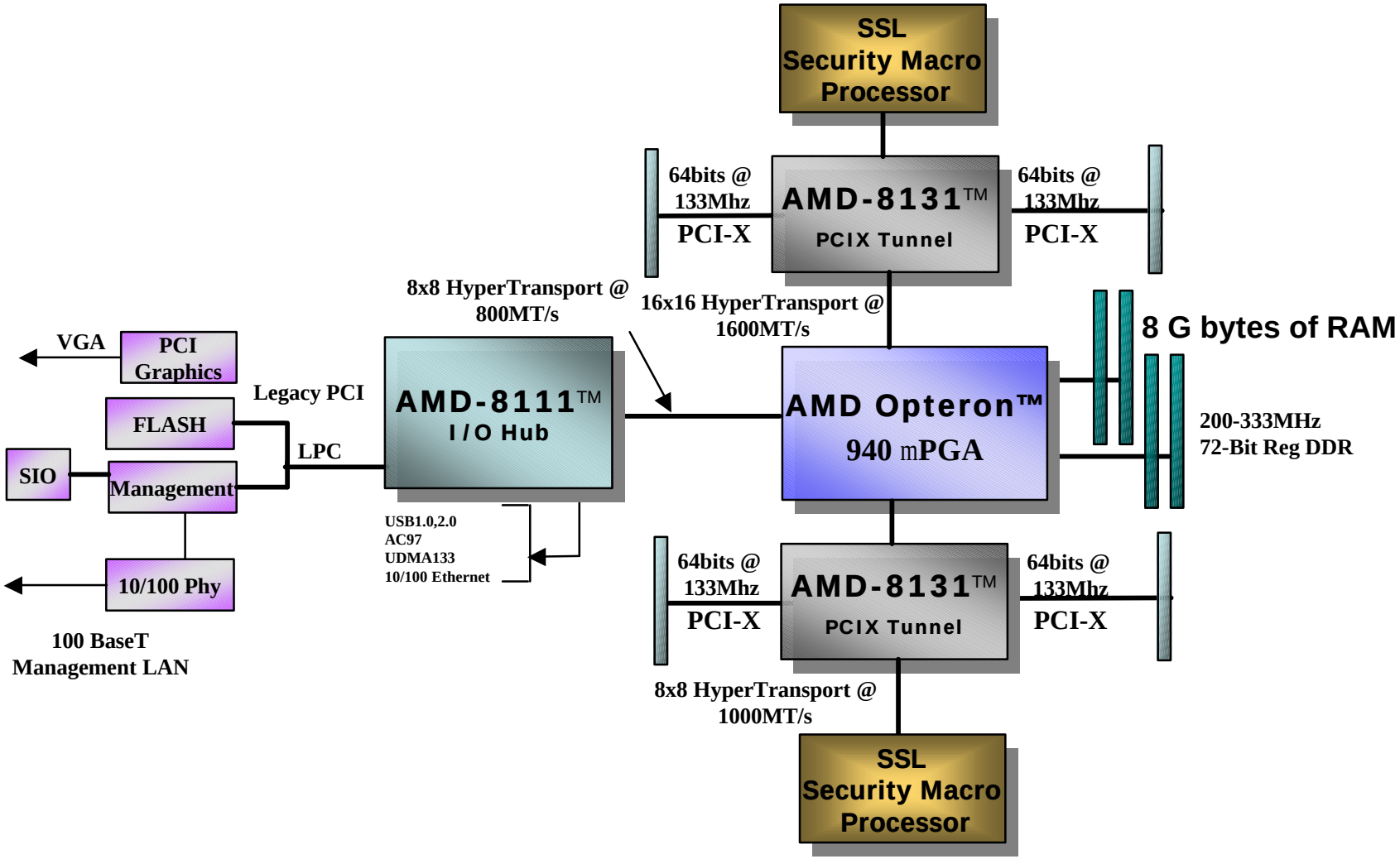
Platform Conference

AMD8131™ in String of Pearl Configurations



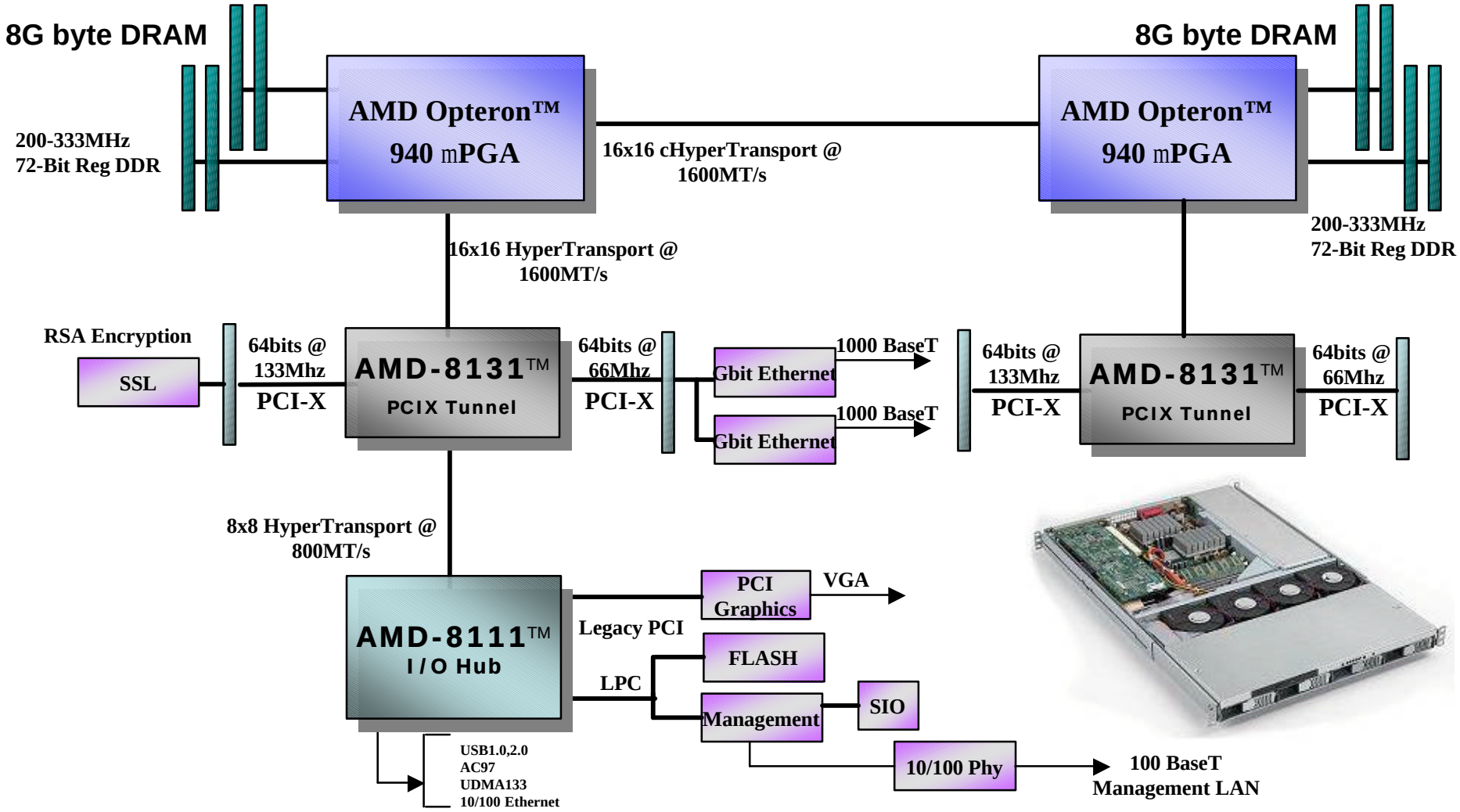
Can add up to 31 I/O devices

AMD Opteron™ 1U/1P Server



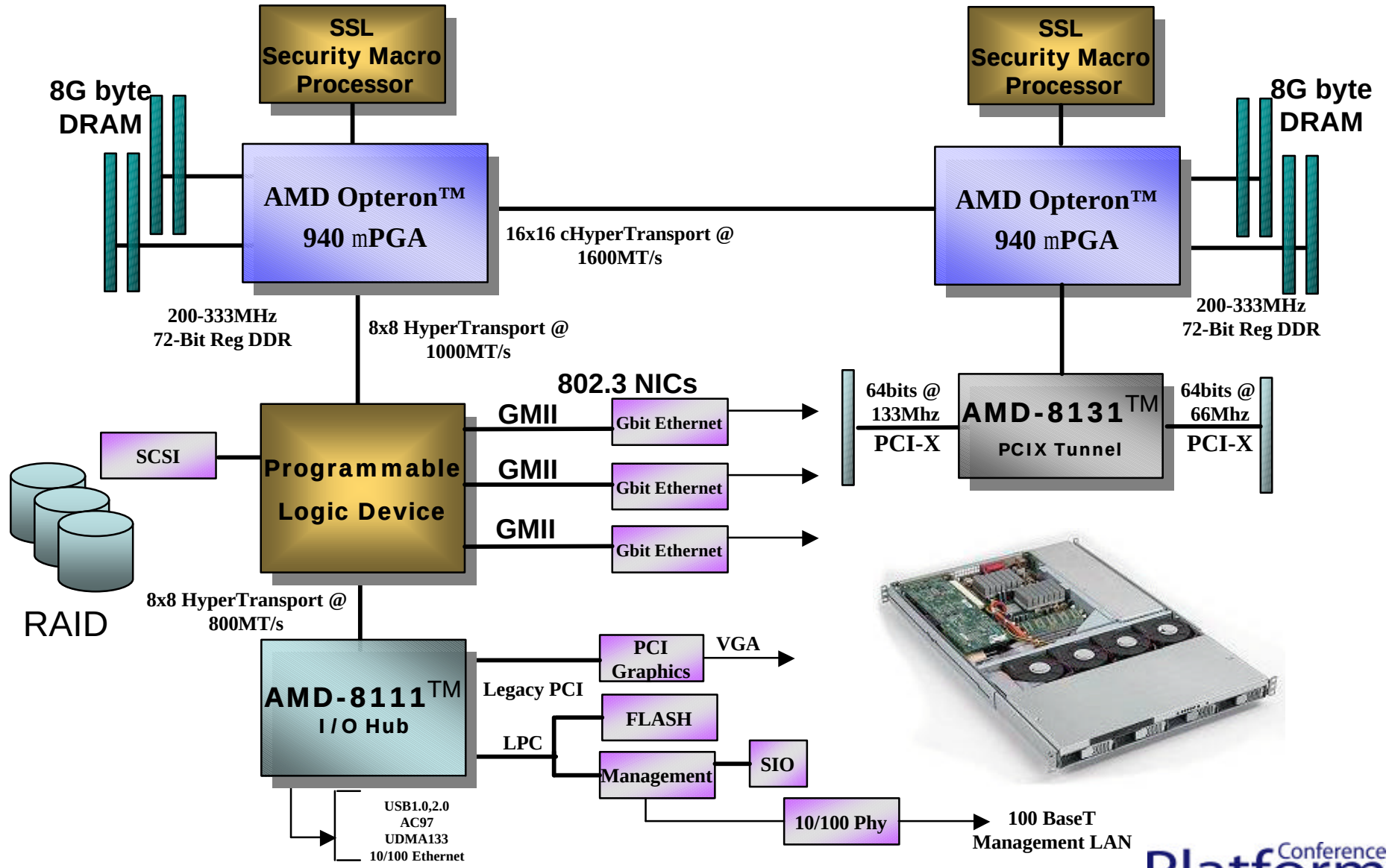
Platform Conference

1U/2P AMD Opteron™ Server



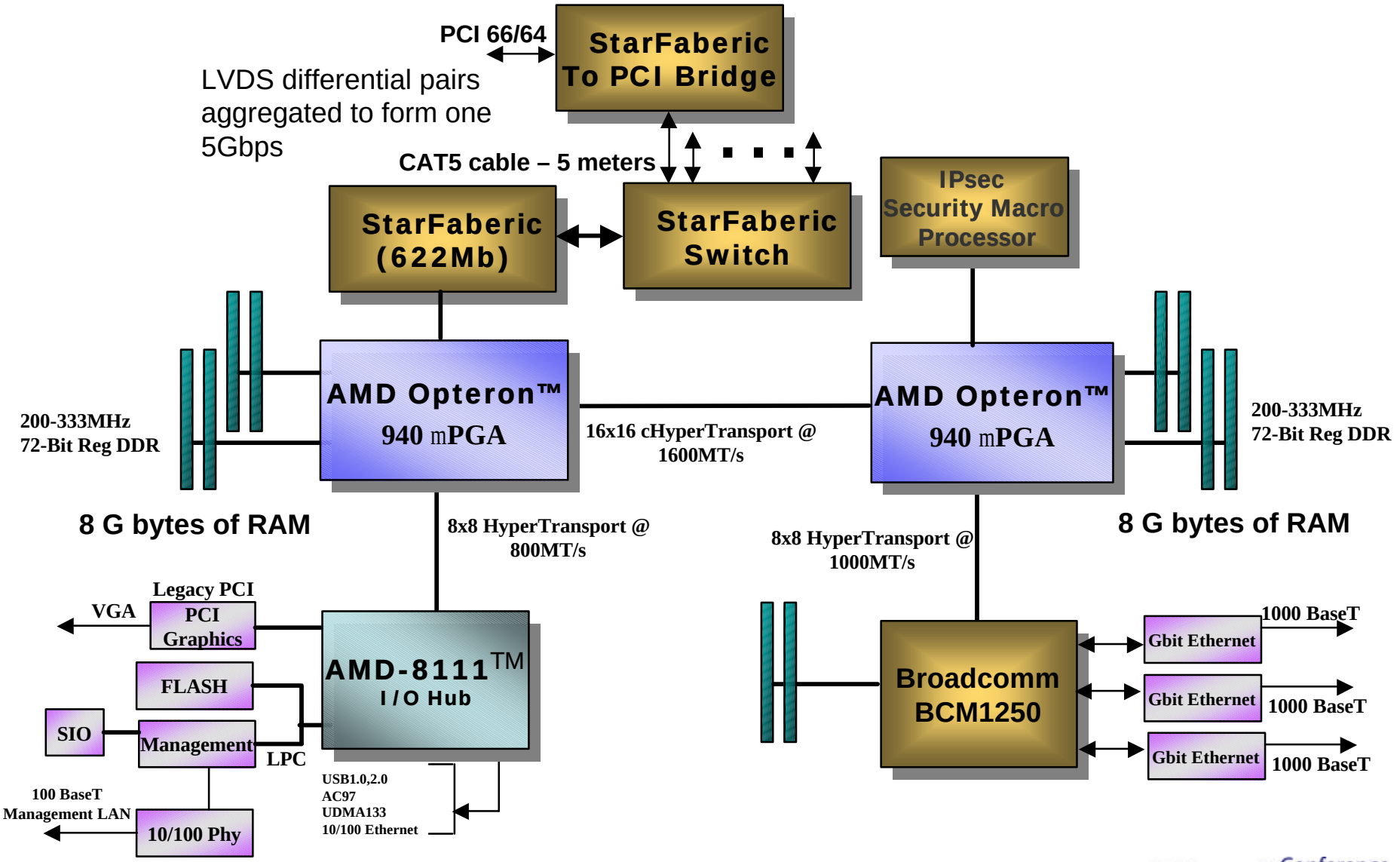
Platform Conference

1U/2P AMD Opteron™ Server



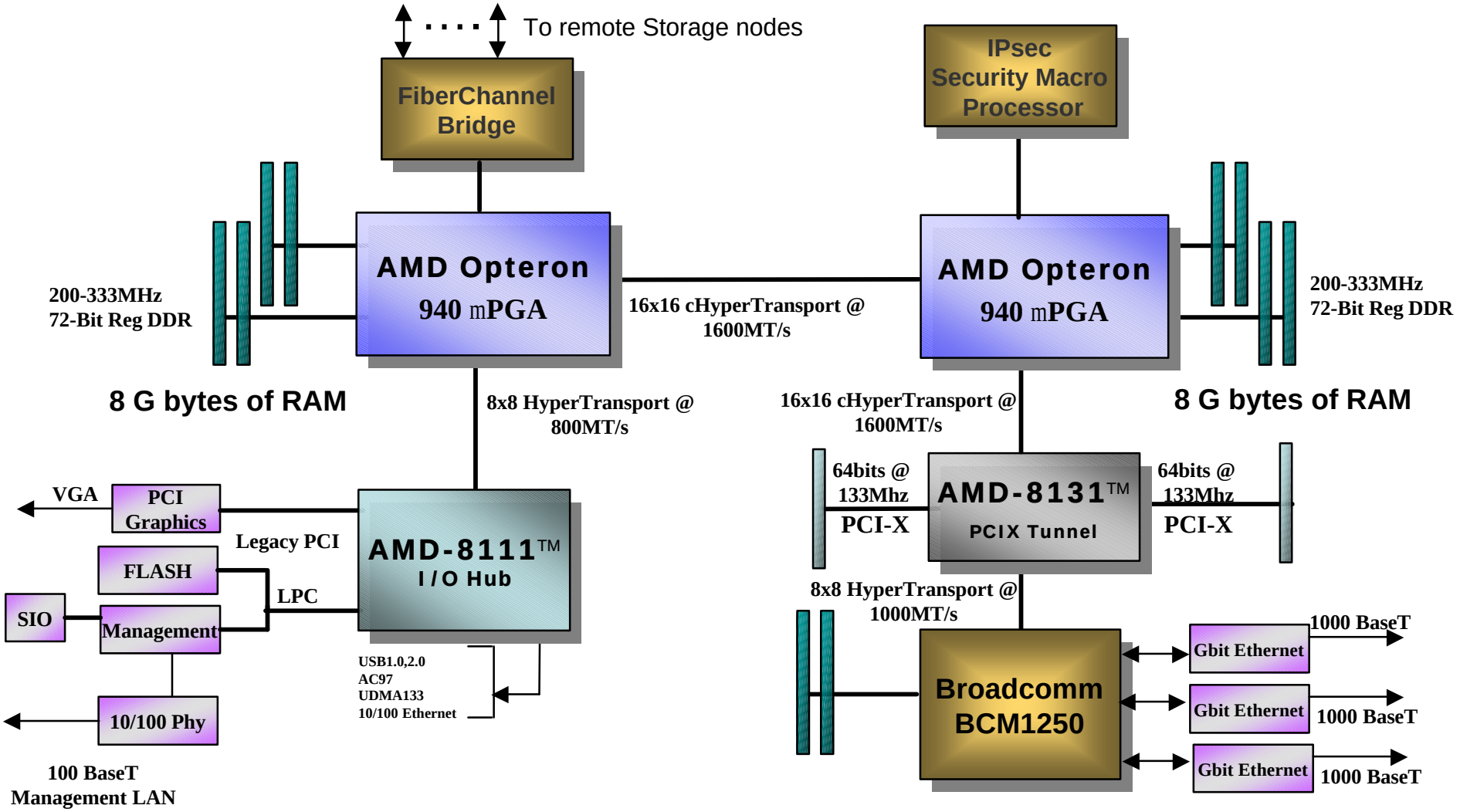
Platform Conference

StarFabric™ Storage Server



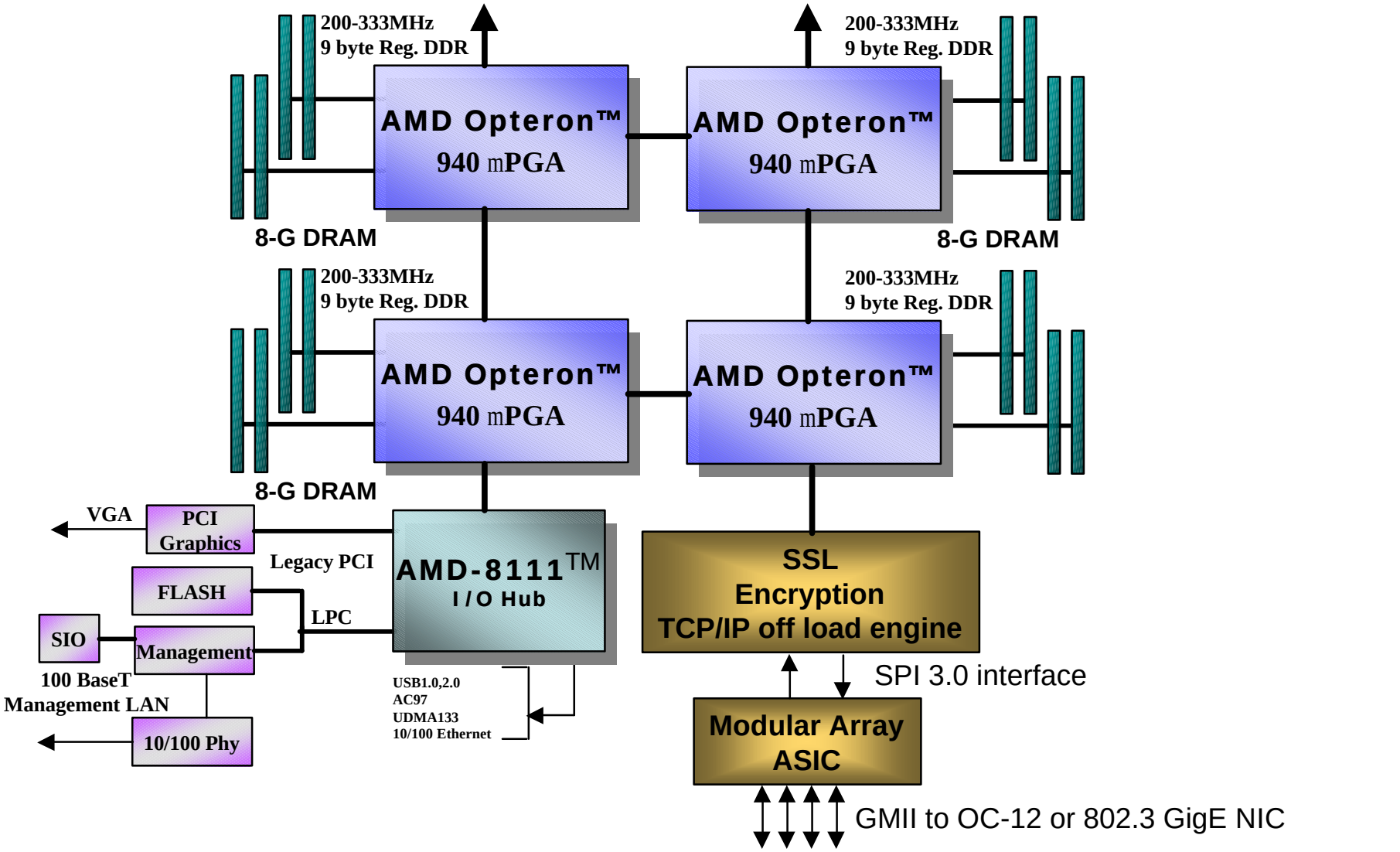
Platform Conference

FiberChannel Storage Server



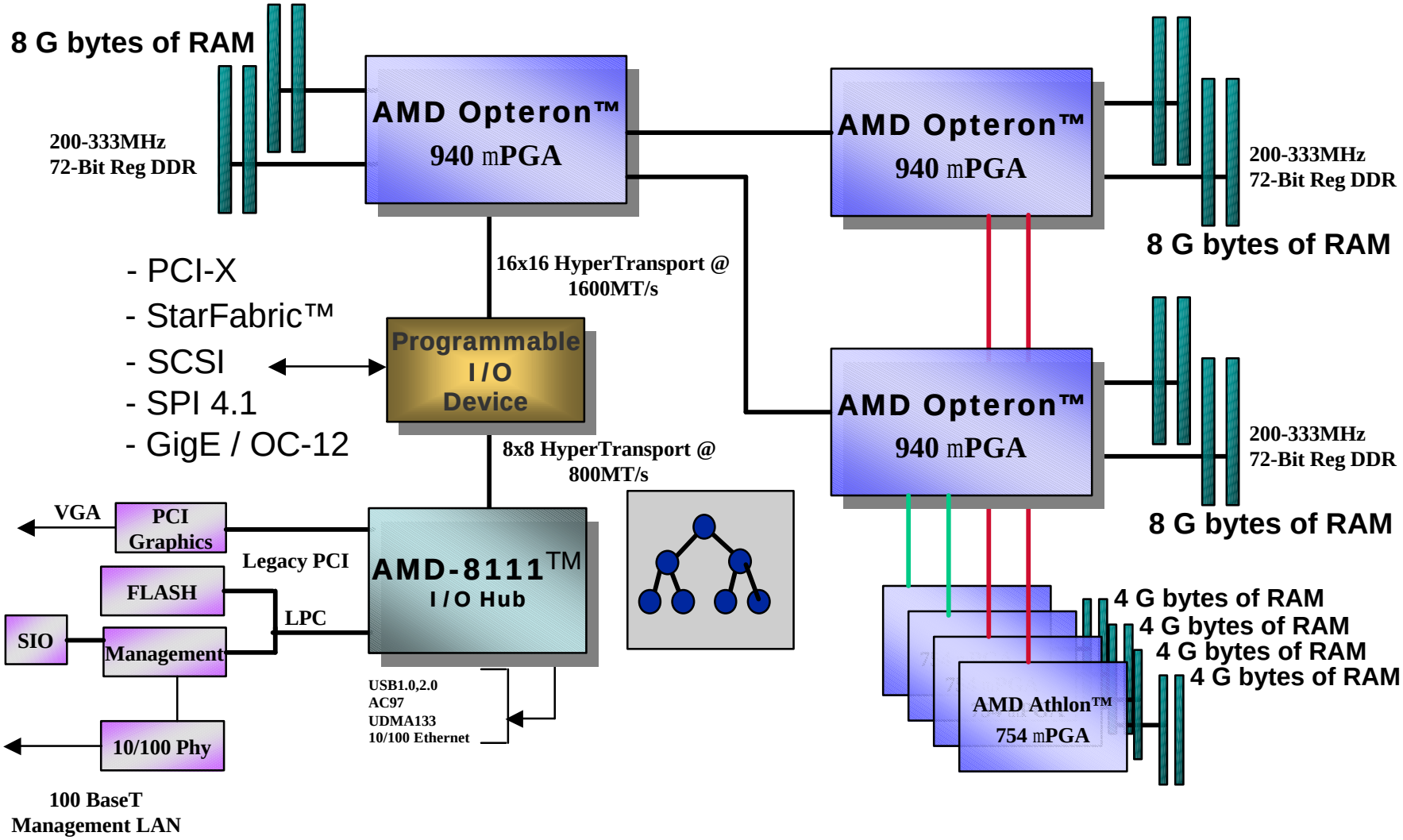
Platform Conference

Quad AMD Opteron™ TCP/IP Offload Engine

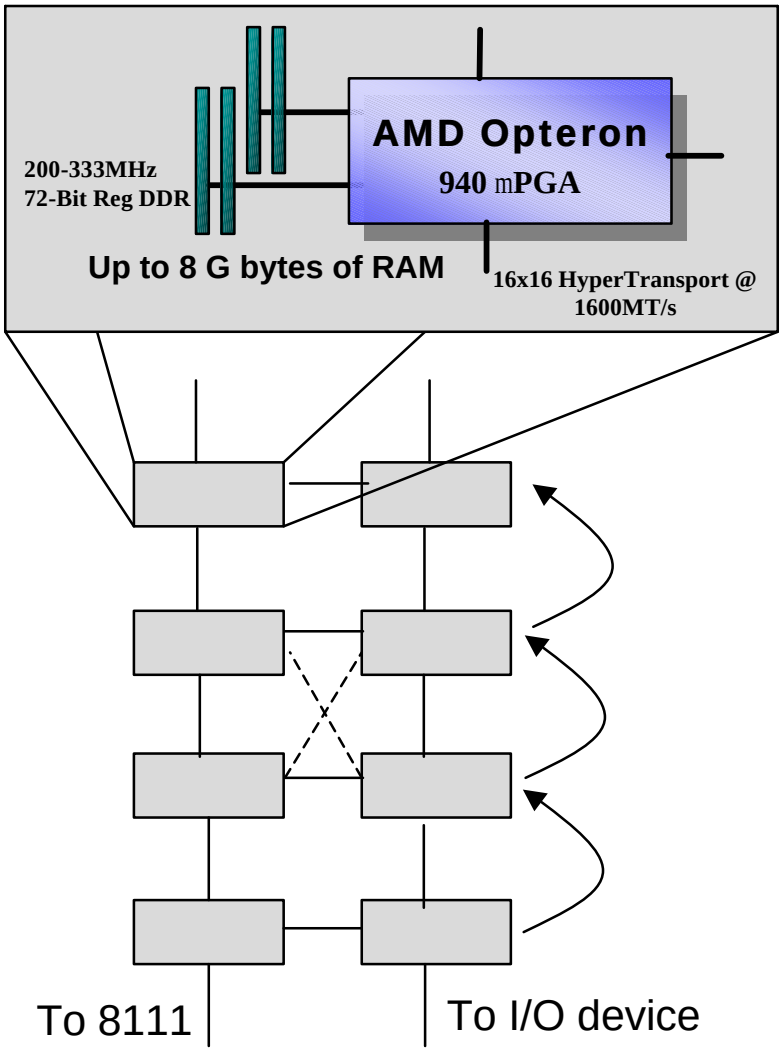


Platform Conference

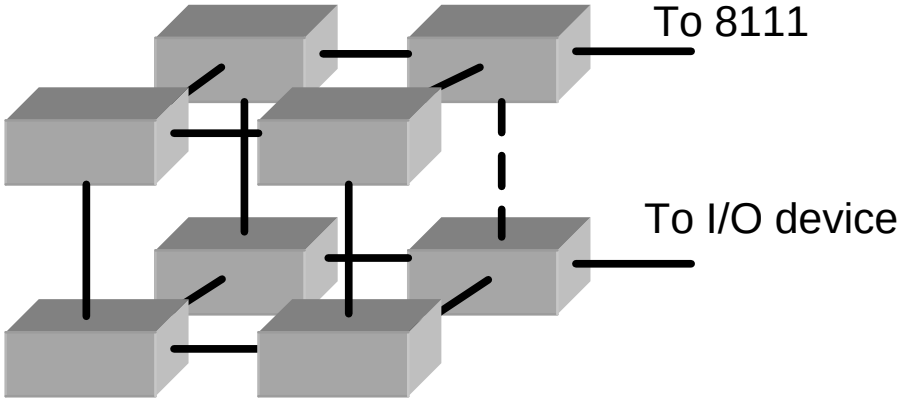
Non-Traditional Topologies
28 G FLOPS Recognition Engine



AMD Opteron™ Cubed – 8P Server Topology



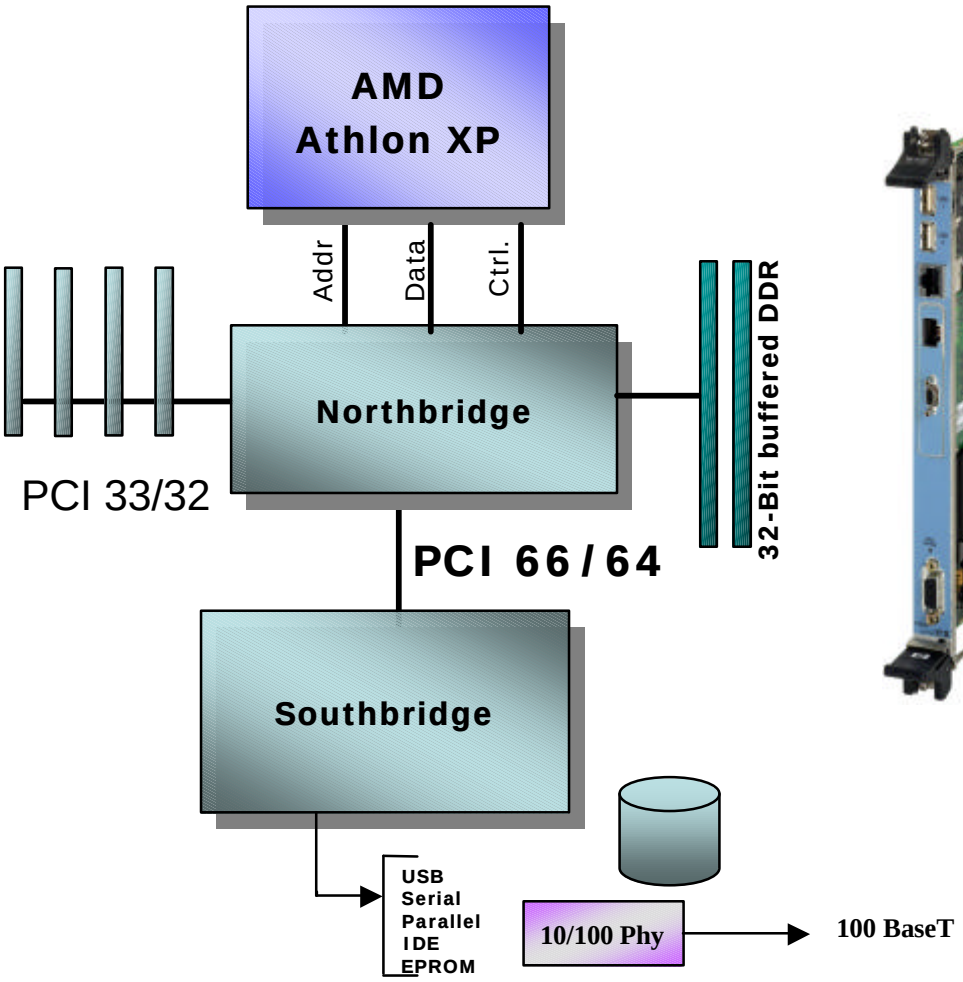
- Only three nodes are 3 hops away
- No nodes are 4 hops away
- More redundant Paths



AMD Athlon™ & AMD Opteron™ Blade Servers

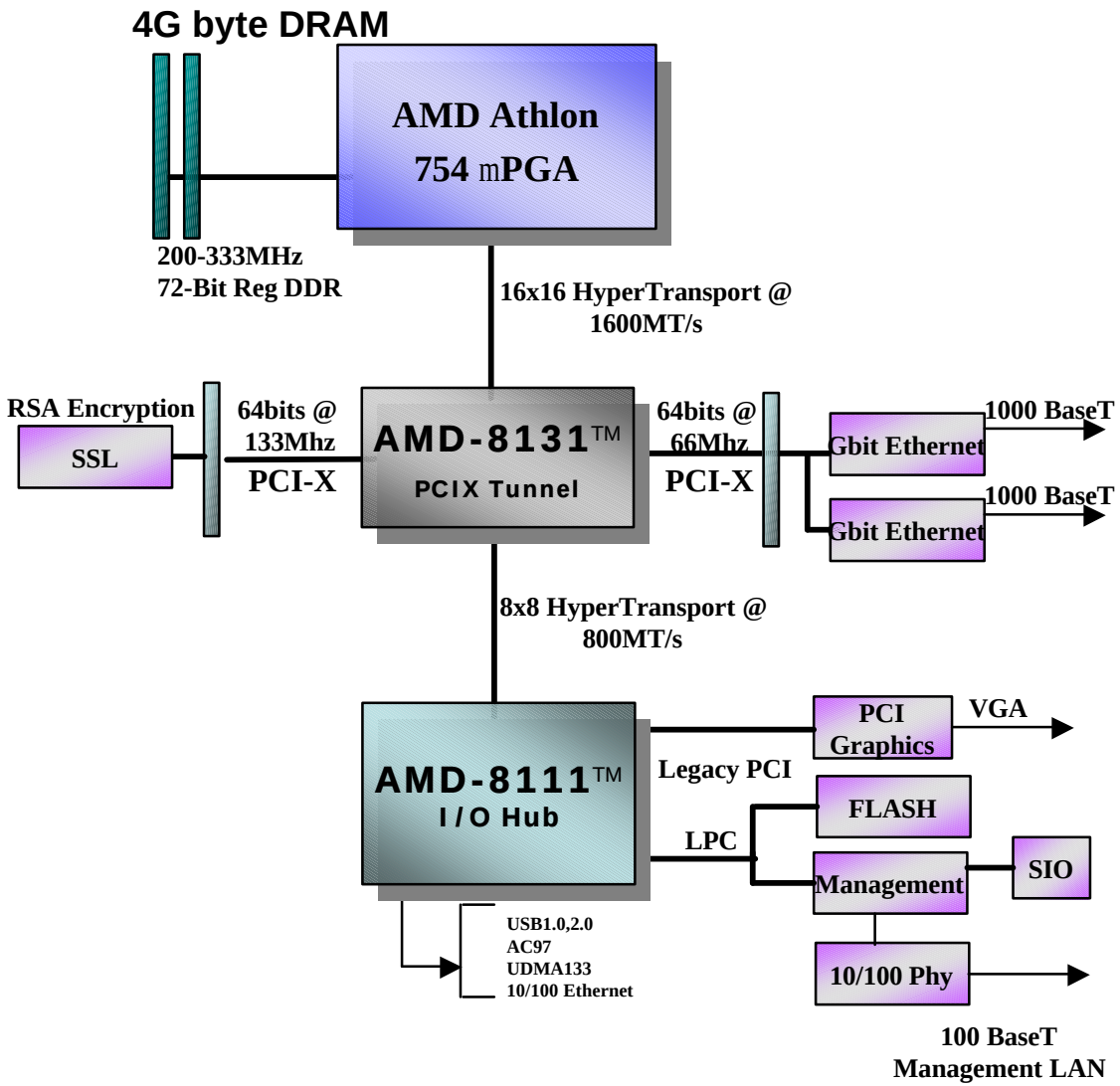
- AMD is participating in major OEM Blade efforts
  - ✓ Establishing an “Open Standard” based on cPCI and HyperTransport
- Many “Value” issues
  - ✓ Power - AMD will offer lower power Hammer
  - ✓ Density - 64-bit computing in Blades
  - ✓ System Management and Fail-Over
  - ✓ Network Management (Interconnects as well as switching)
  - ✓ Scale-Out & hot-Swap
- Next Generation Applications
  - ✓ Storage Area Networks (SAN)
  - ✓ High Performance Computing (HPC)
  - ✓ Mobile Telephone Switch Office (MTSO)
  - ✓ On Demand Content Delivery (ODCD)
  - ✓ Recognition engine
- Possible future chipset directions to optimize Blades
  - ✓ Integrated OC-48
  - ✓ Integrated TCP Offload Engines (TOE)
  - ✓ Integrated dual processor

Traditional 2P Blade Server



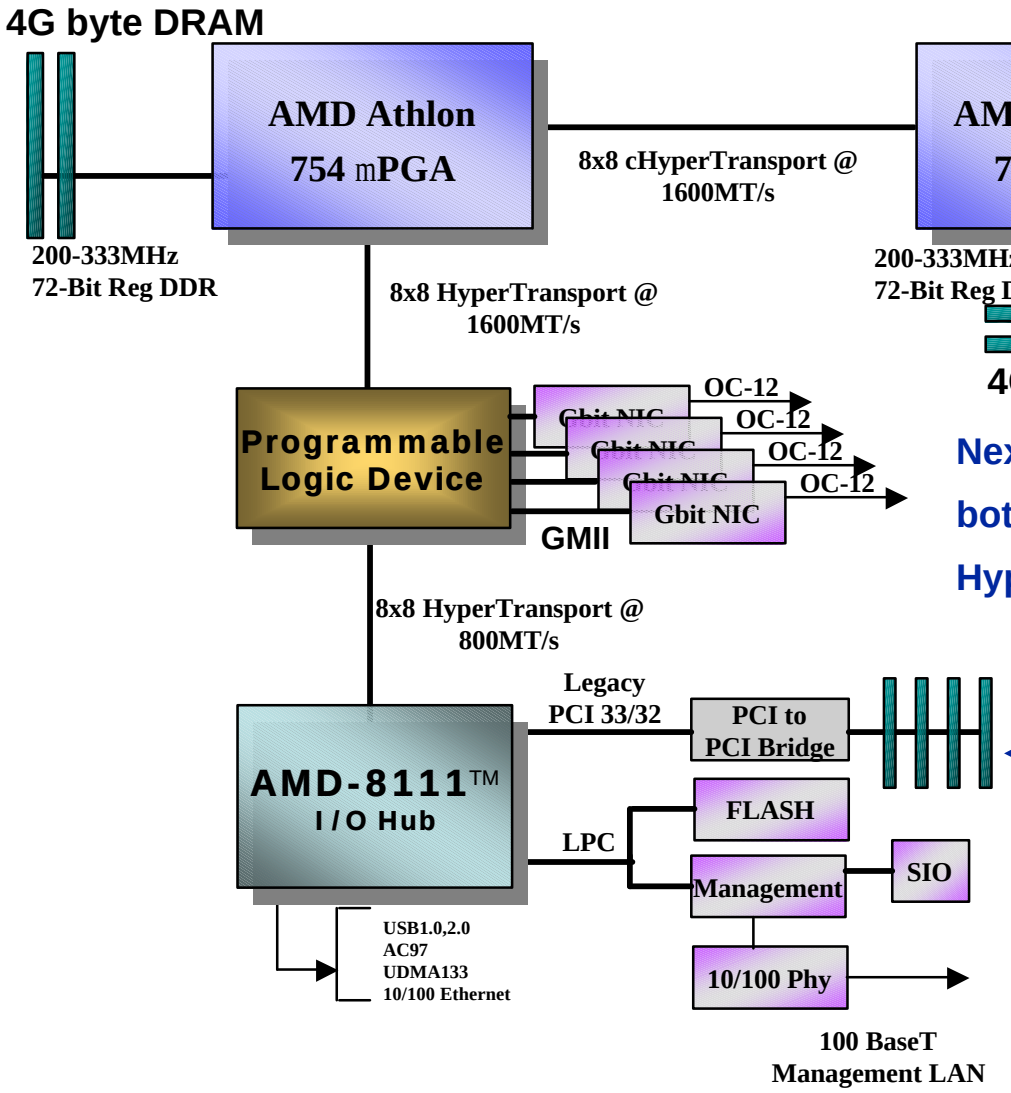
- Blade server limited to Control Functions due to limited bandwidth and throughput
- Not possible to support 4P or even 2P server topology.
- Limited local RAM
- No way to off-load the HDD

AMD Athlon™ 1P Blade Server



- High bandwidth and throughput. Capable of addressing both the Control and Data Plane Functions
- PCI-X & PCI 33/23 Hot swap support (P2P bridge needed for 33/32 Hot swap support)
- With HDD removed, room for 2P or even 4P server topologies.
- Up to 4G bytes of local RAM

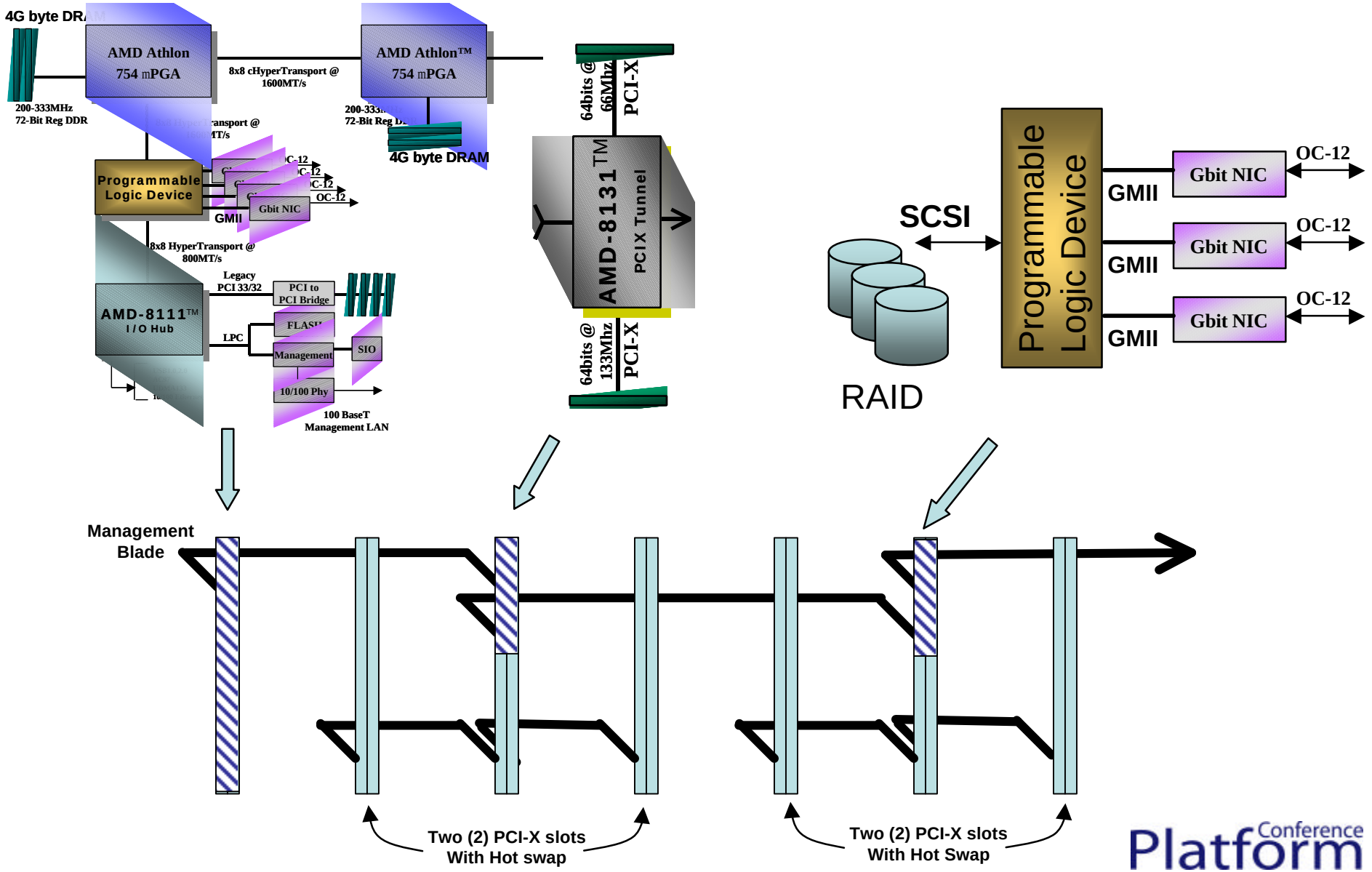
HyperTransport on the Back-Plane
AMD Athlon™ 2P Blade Server



Next generation of Blade Server can now support both a legacy PCI interface as well as an 8-line HyperTransport interface on the back plane

Platform Conference

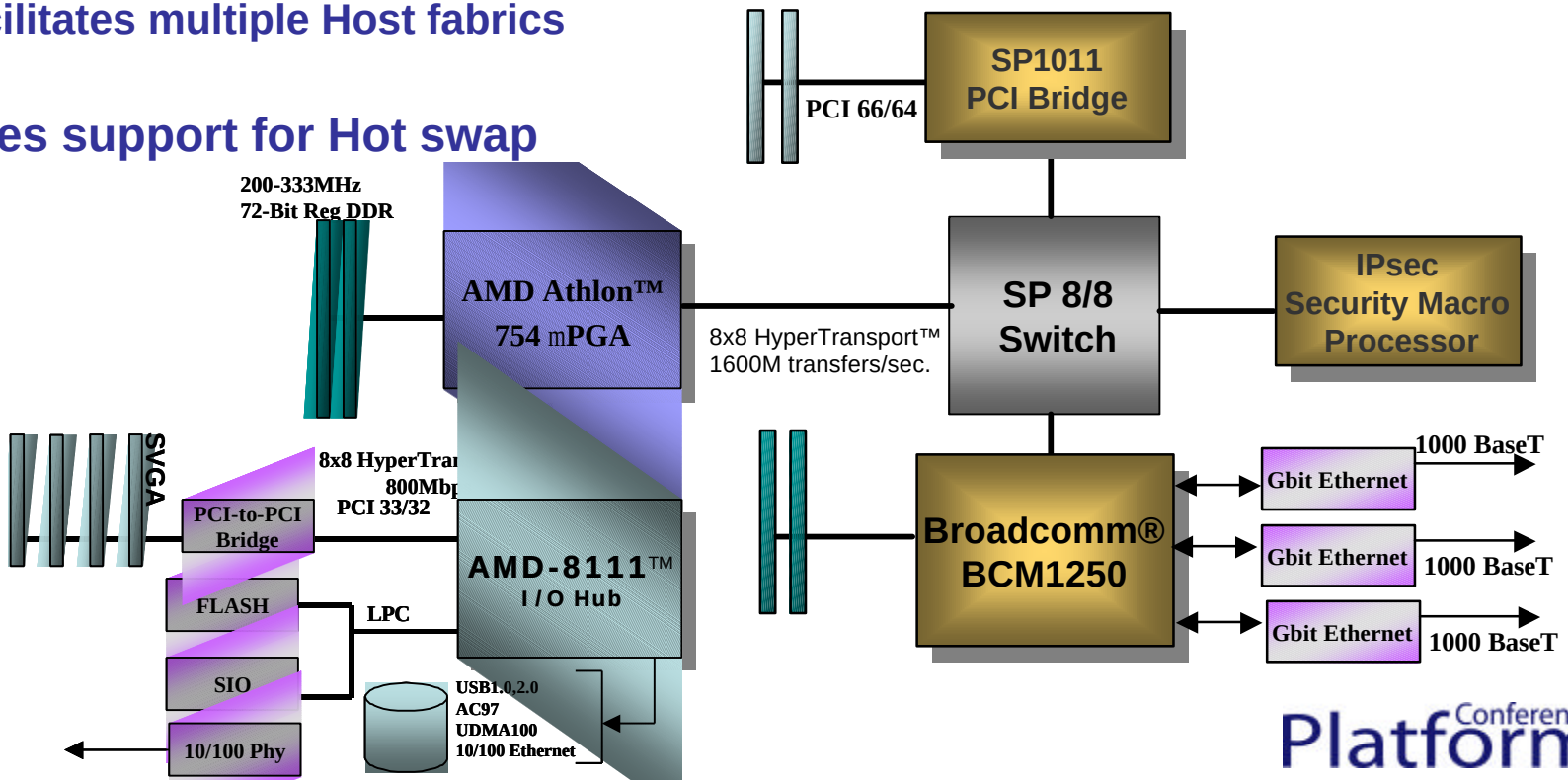
AMD Opteron™ Facilitates a Hybrid Modular Blade Server



Platform Conference

HyperTransport ™ Switch

- Extends the fabric by re-mapping Unit_IDs at each port
  - ✓ Tracks path of packet that pass through it, guaranteeings the same return path
  - ✓ Records the incoming Unit_ID so it can be restored in the response packet
- Follows same rules as Processor Host interface
  - ✓ Peer-to-peer through the switch freeing up the host
  - ✓ Facilitates multiple Host fabrics
- Provides support for Hot swap



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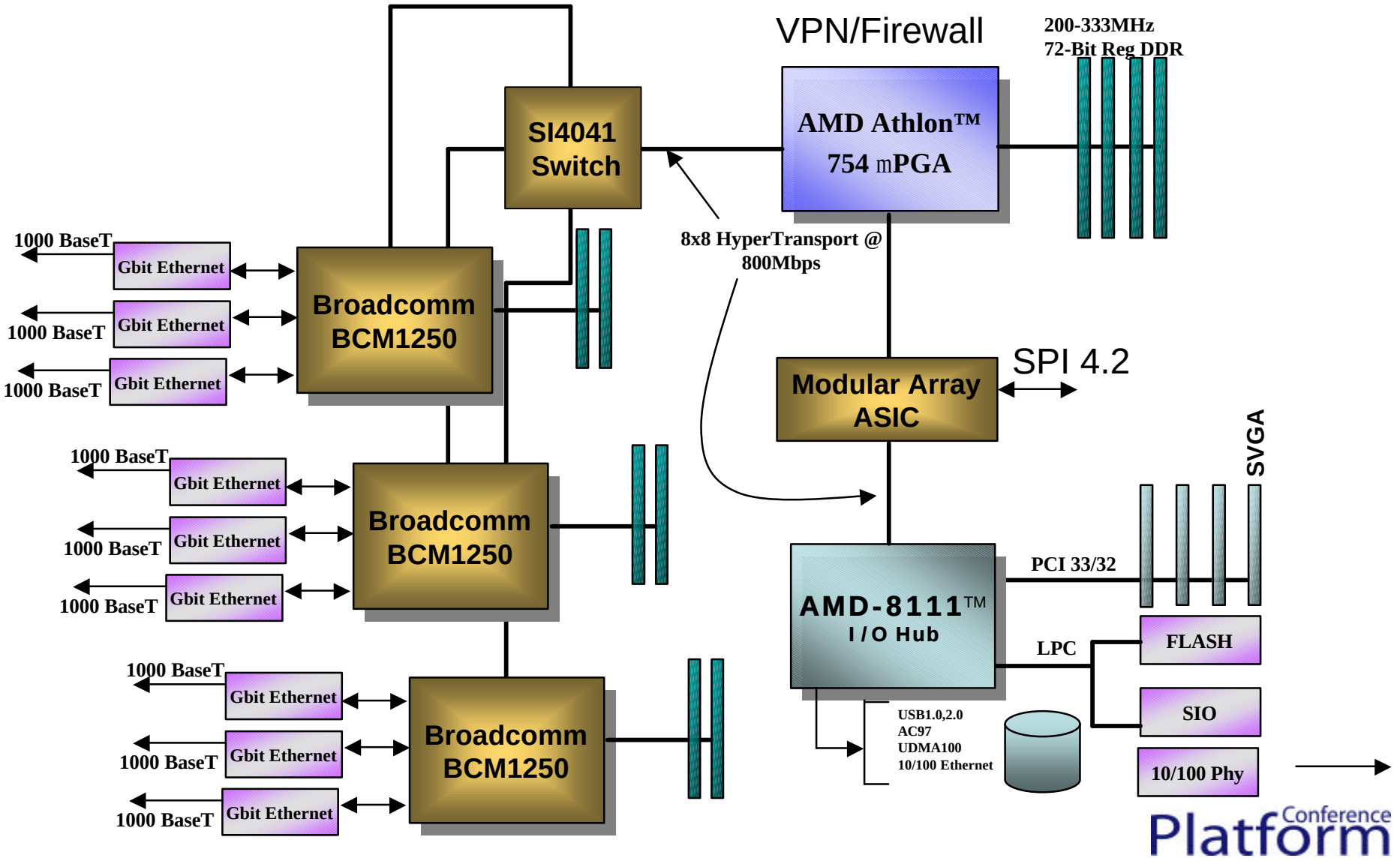
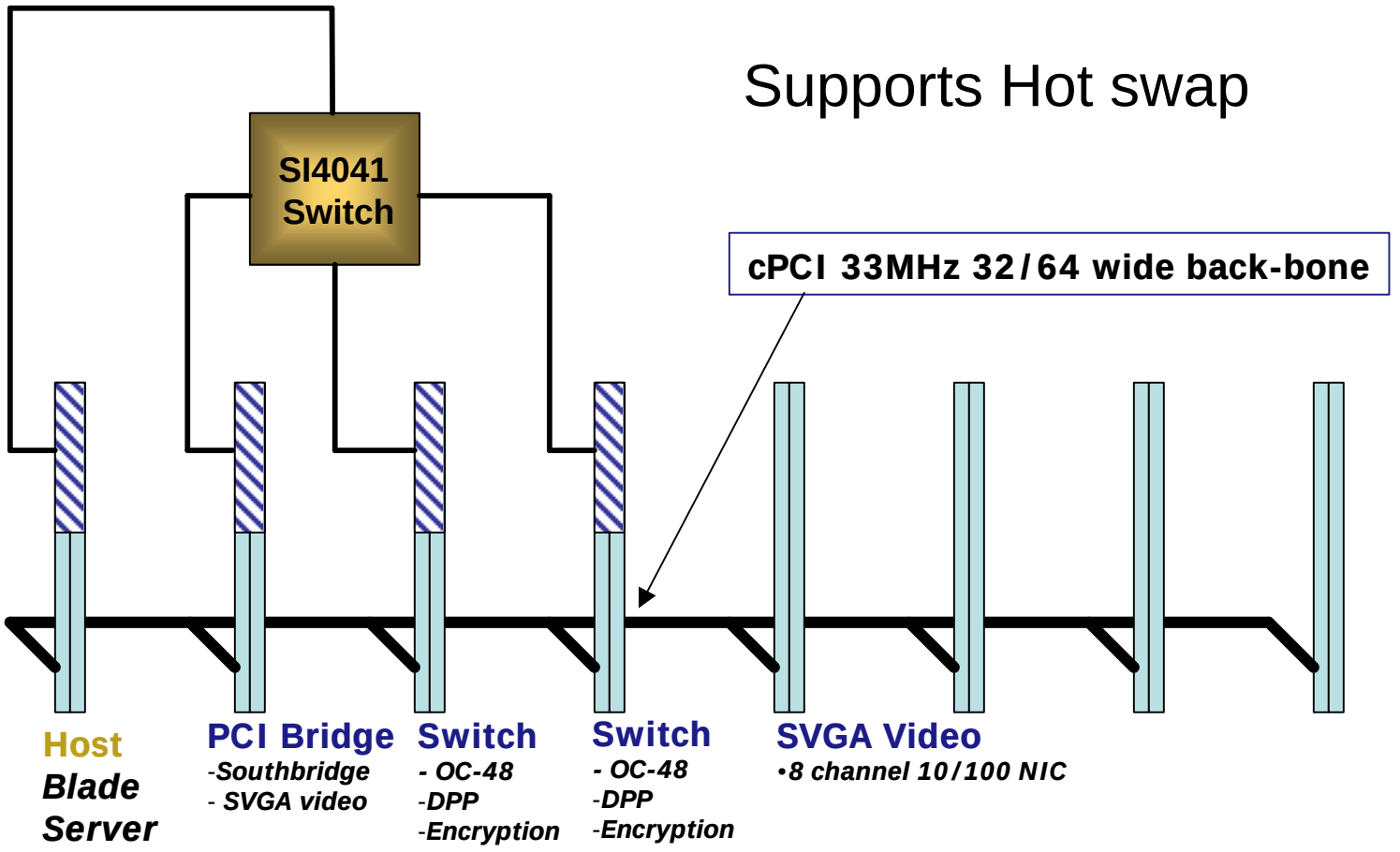
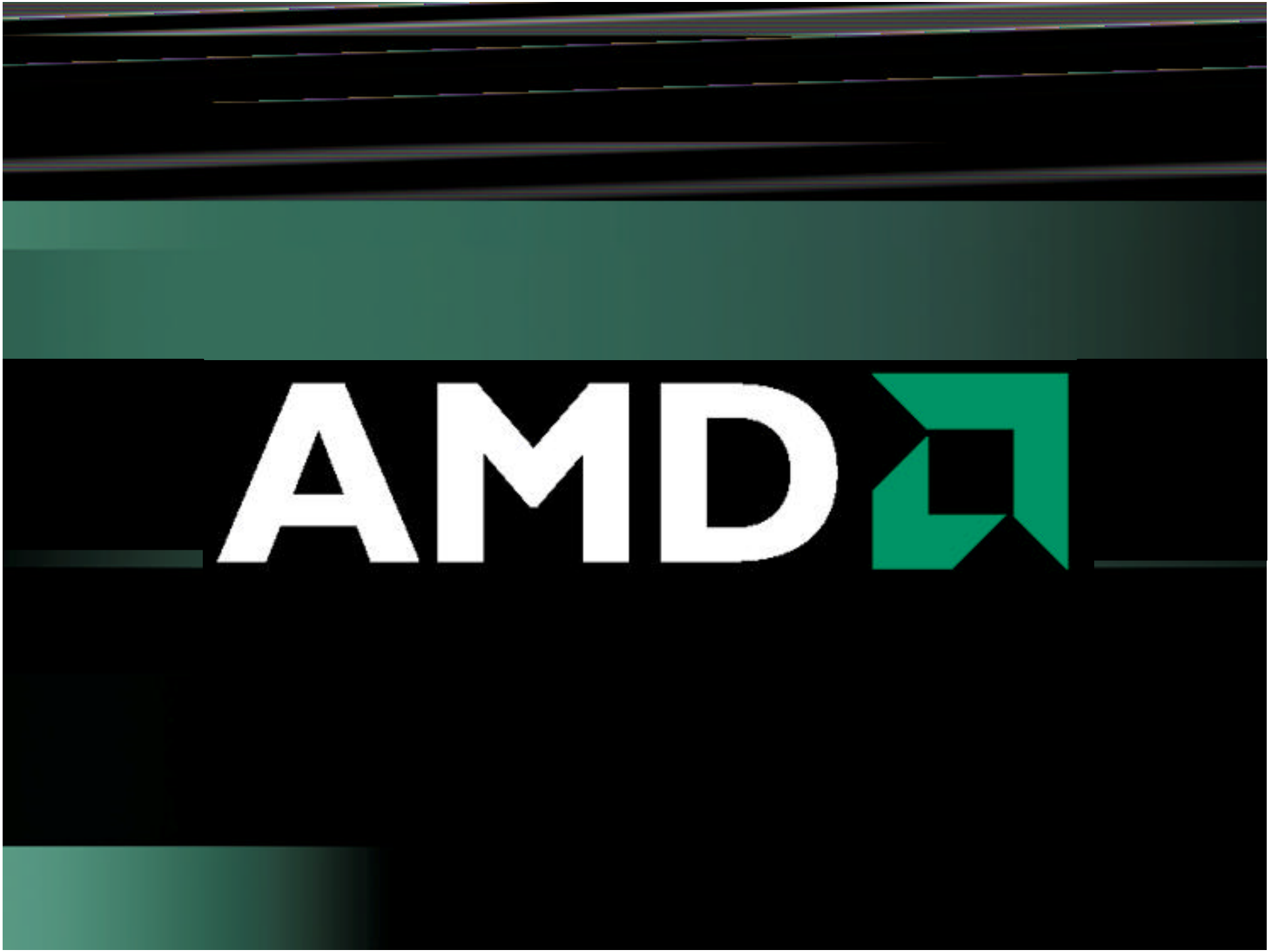
Nine channel GigE Firewall



HyperTransport™ Back-Plane With a Switch




AMD